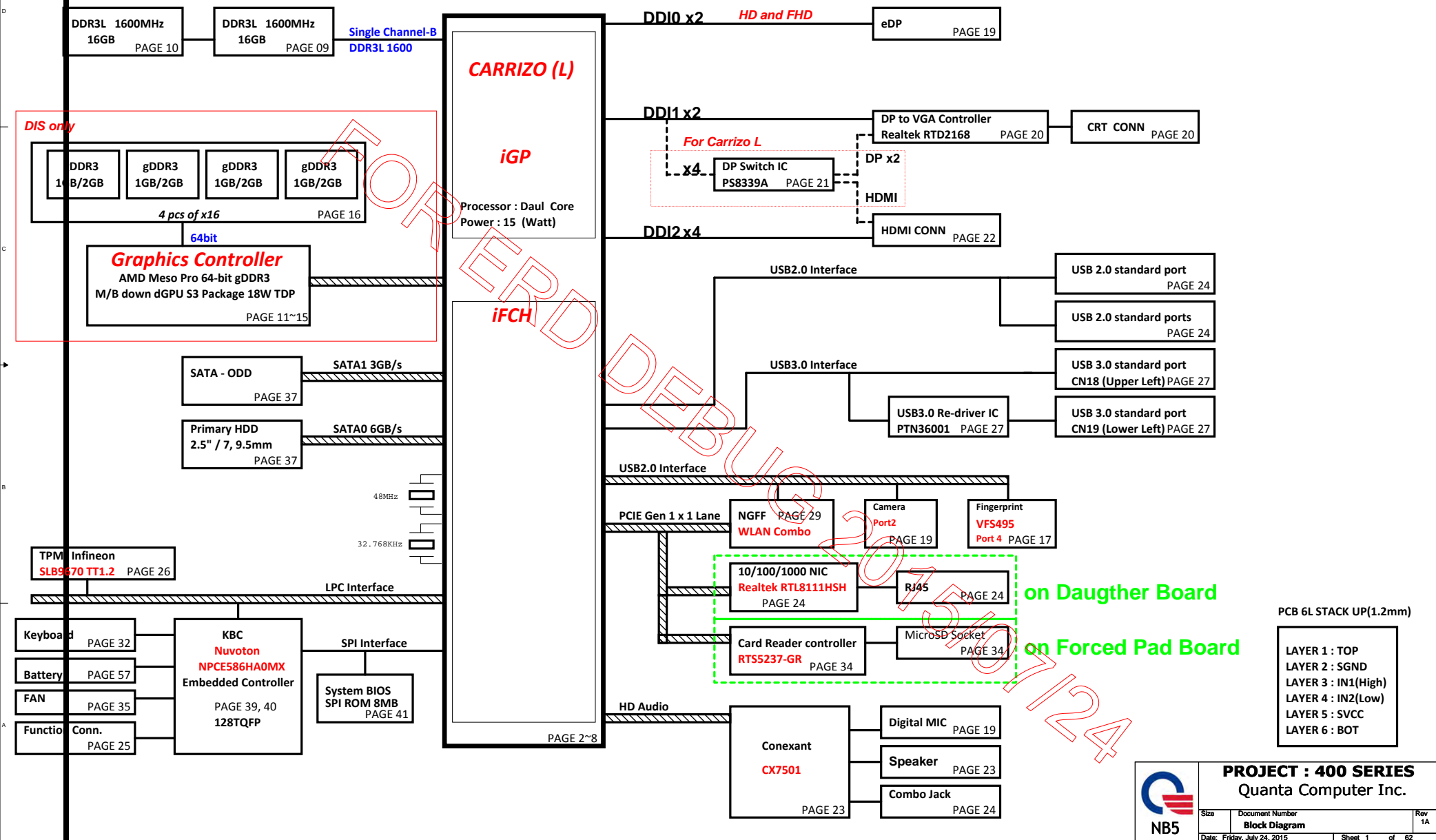
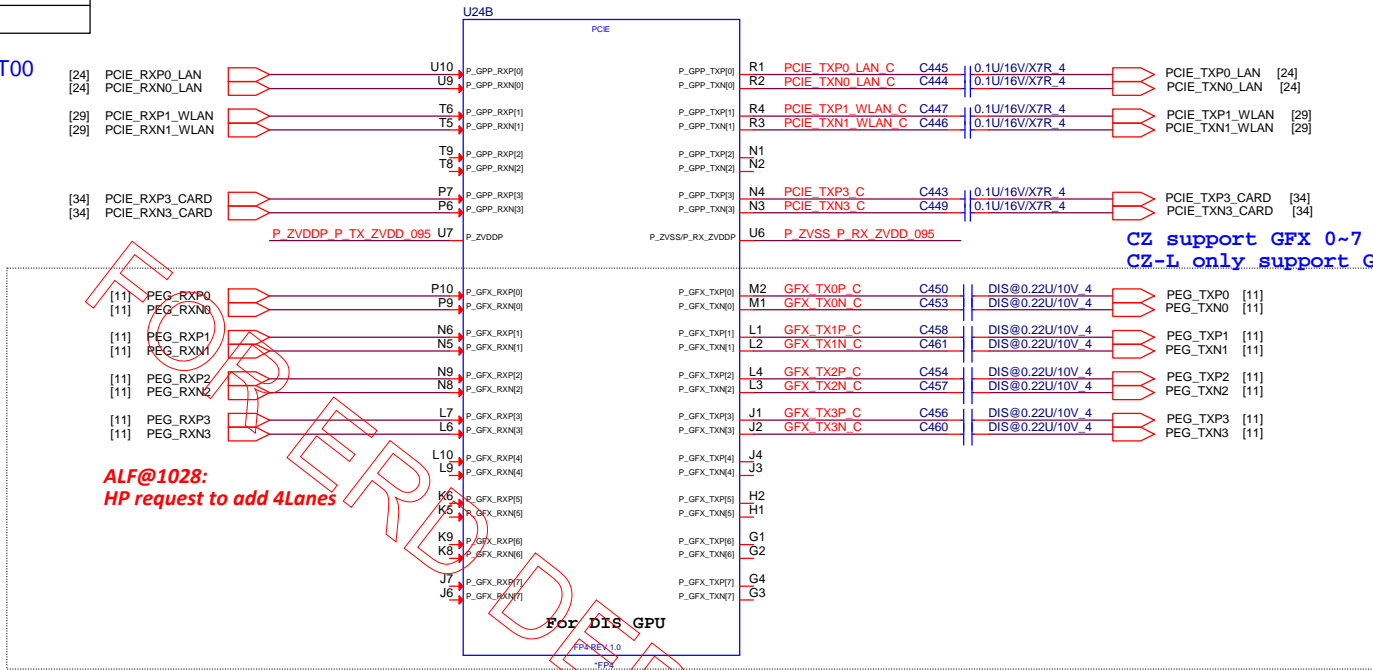


400 series Palazzo / X73A (UMA/DIS) Schematics



	QBCON	TOPBSQ
Carrizo	AJ1802CUT01	AJ1802CUT02

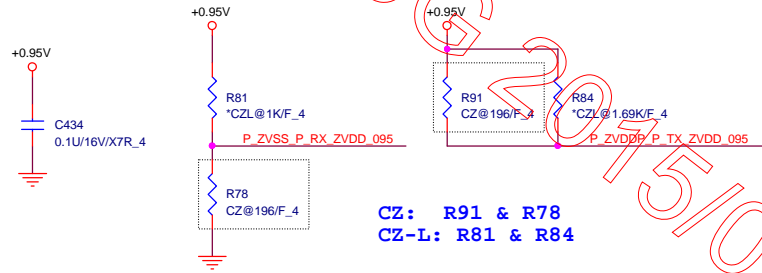
Carrizo DB phase use AJ1802CUT00



CZ support GFX 0~7 & Gen3
CZ-L only support GFX 0~3 & Gen2

ALF@1028:
HP request to add 4Lanes

Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4103K1B08

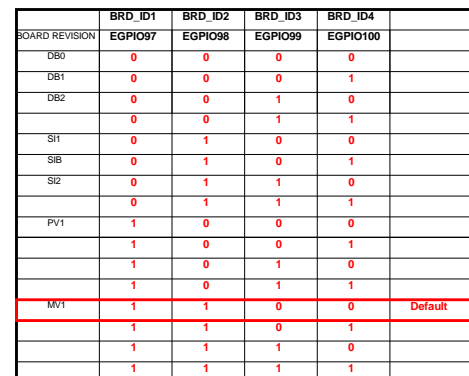


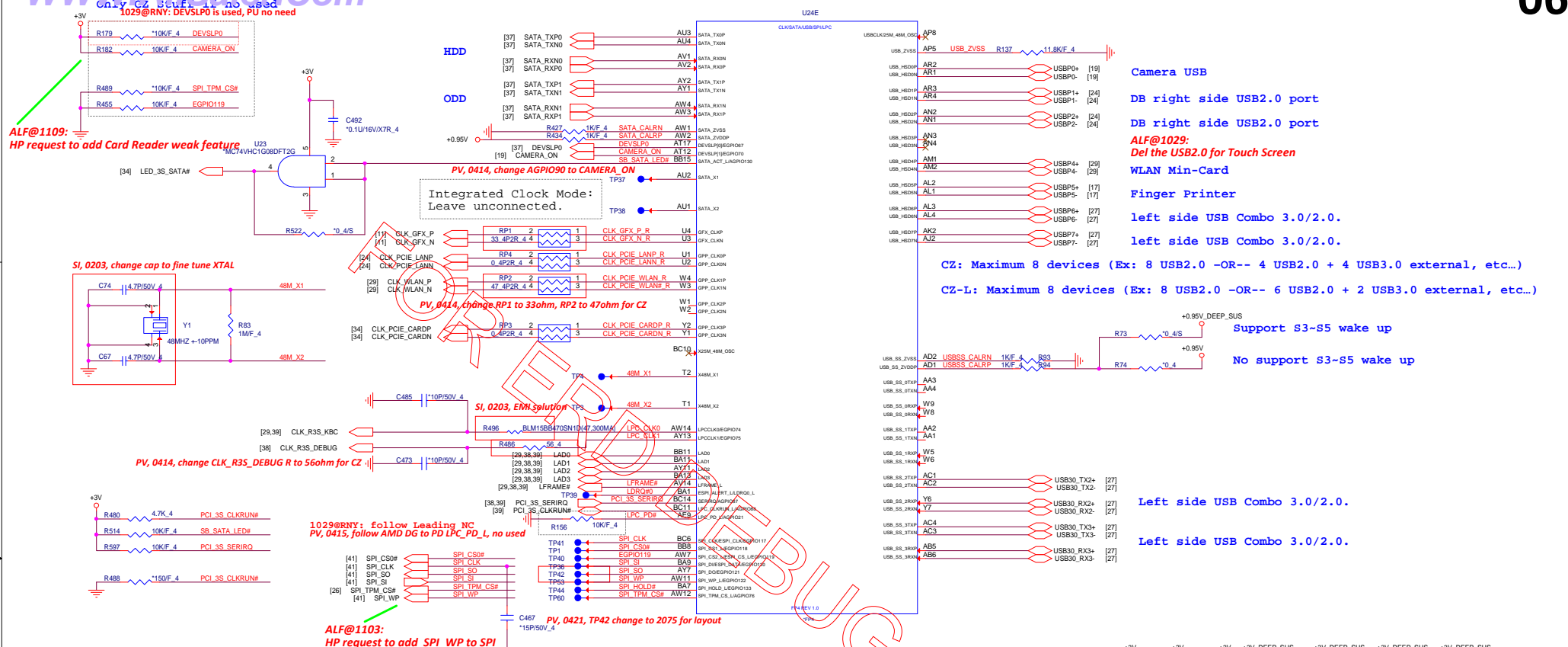
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
	Carrizo 1/7 (PCIE)	1A
Date: Friday, July 24, 2015	Sheet	of 62

1102@RNY: AMD recommend reserve test point at VREFDQ/ZVDDIO MEM S







STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

1024@Ronny: AGPIO11 STRAP?

CZ: pop R445
CZ-L: pop R457

Follow FAE comment: R659 change to 2K, R401 to 10k, R142 is NC

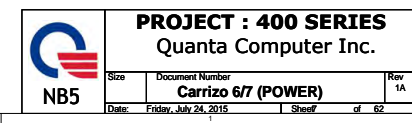
REQUIRED STRAPS

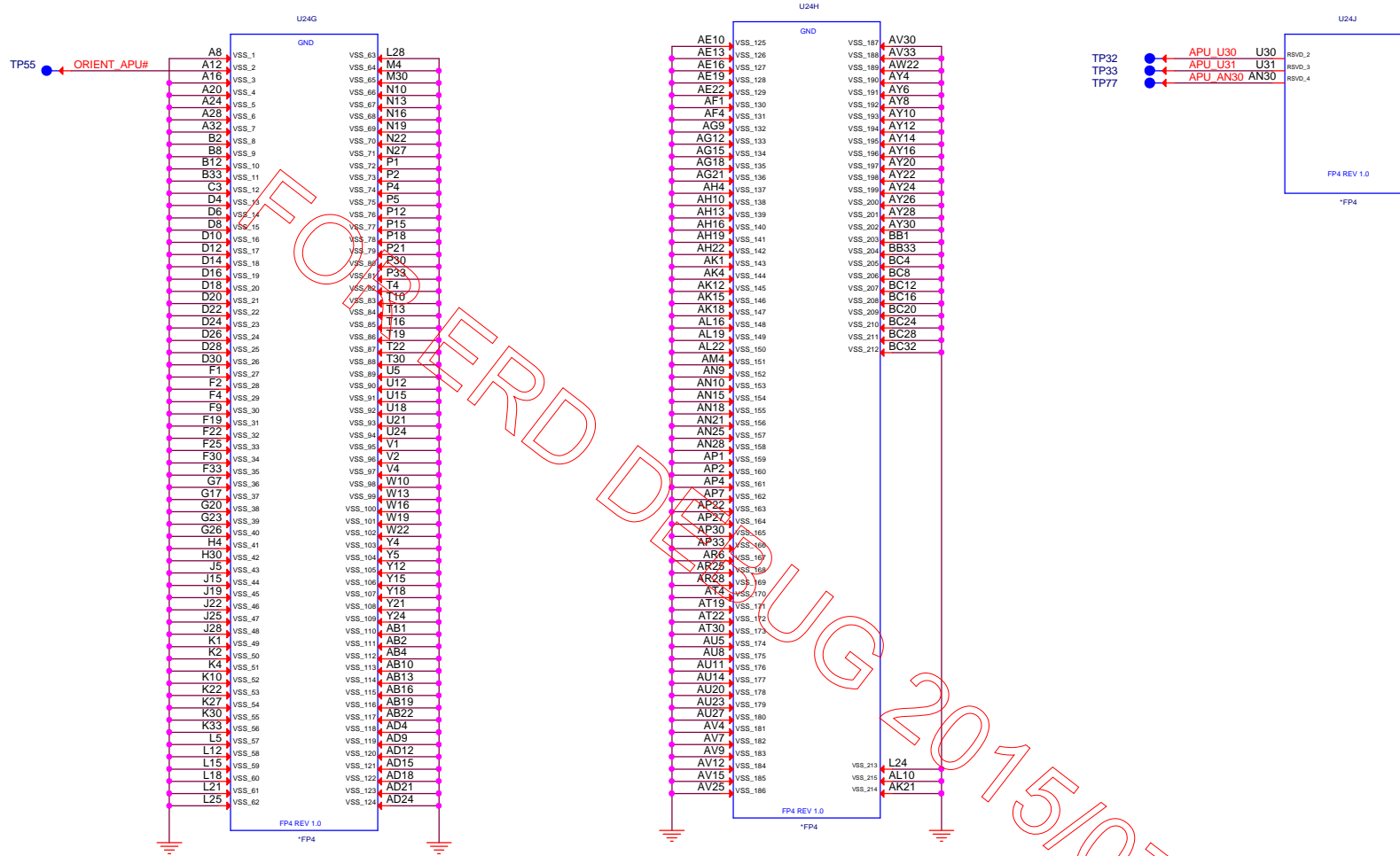
	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 Init Pull-Up	RTC_CLK Init Pull-Up	AGPIO11 Init Pull-Up	SYS_RST# Init Pull-Up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM DEFAULT	Coin battery is on board. DEFAULT	LDT_RST#LDT_PWRGD output to APU output to Pads DEFAULT	normal reset mode DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100MHz PCIe clock as reference clock and generate internal clocks only	LPC ROM	3.3V SPI ROM Default to traditional reset logic	Coin battery is not on board.	LDT_RST#LDT_PWRGD output to Pads	short reset mode



PROJECT : 400 SERIES
Quanta Computer Inc.

Size Document Number Carrizo 5/7 (SATA/USB/SPI) Rev 1A
Date: Friday, July 24, 2015 Sheet 6 of 62



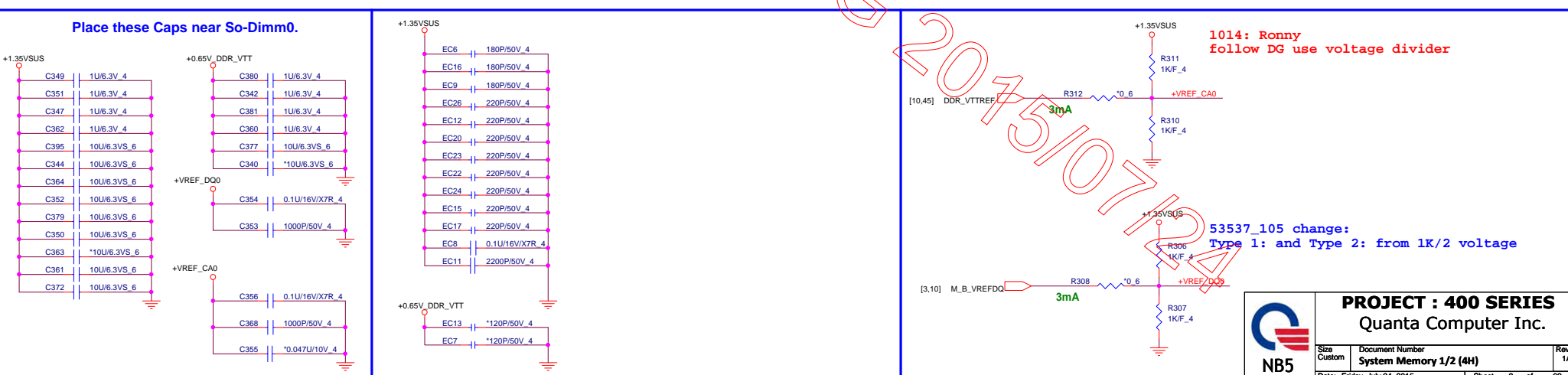
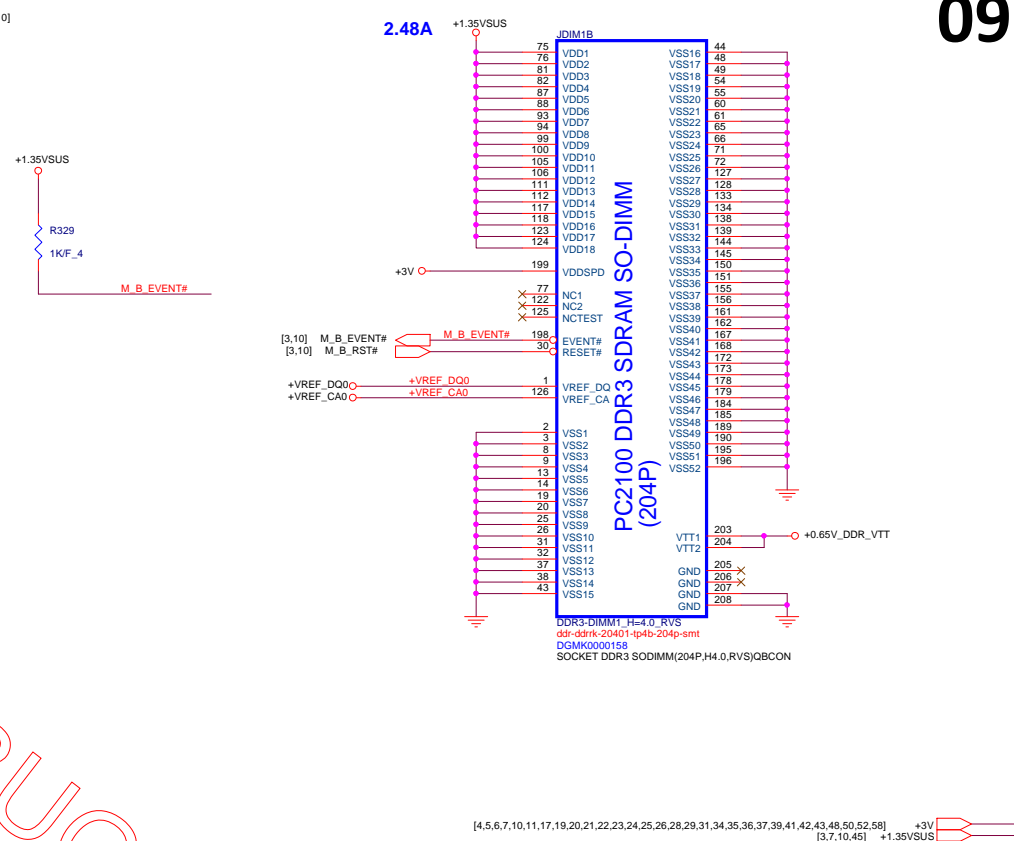
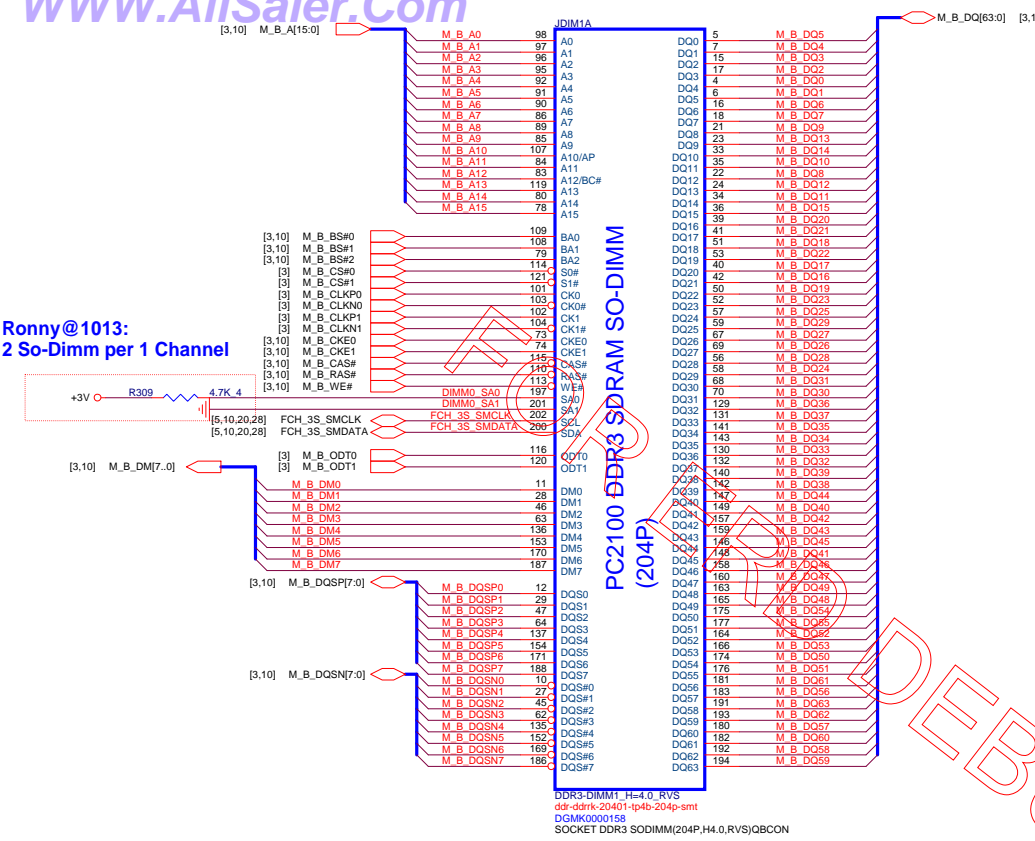


NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

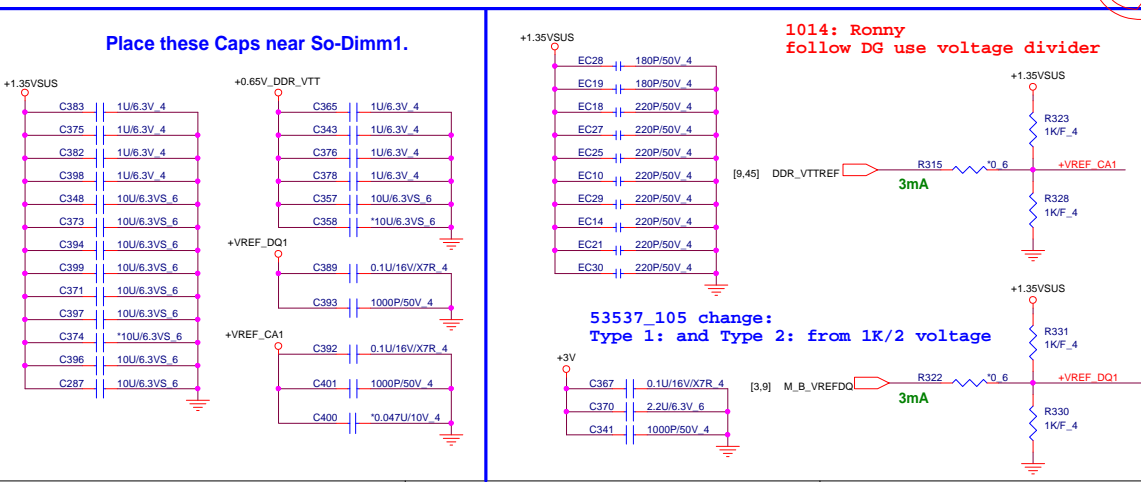
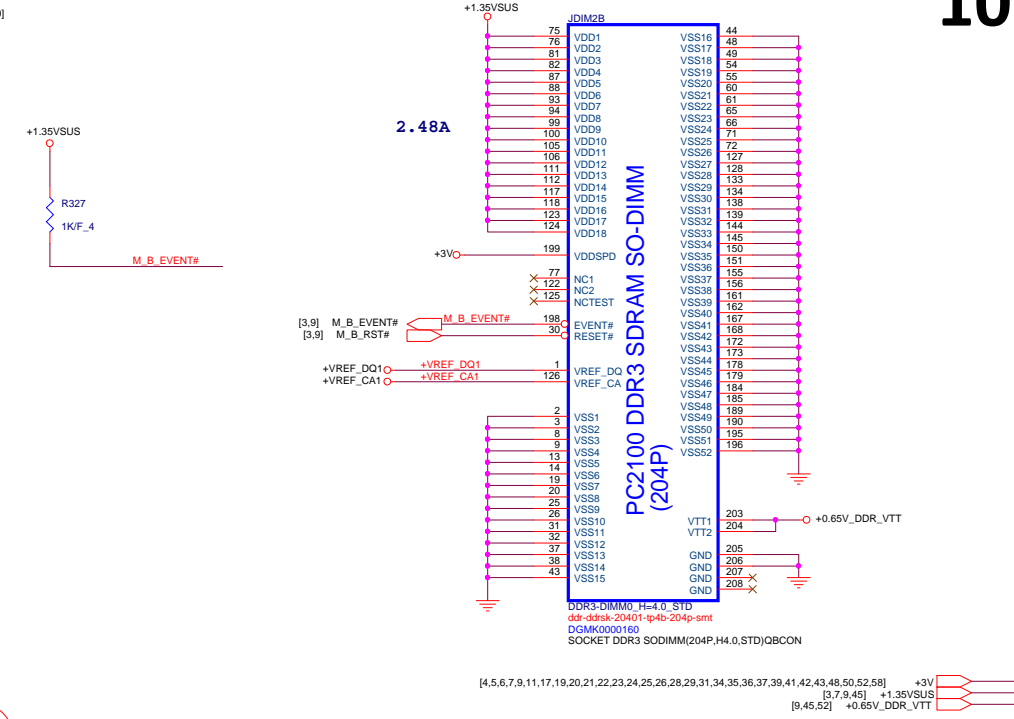
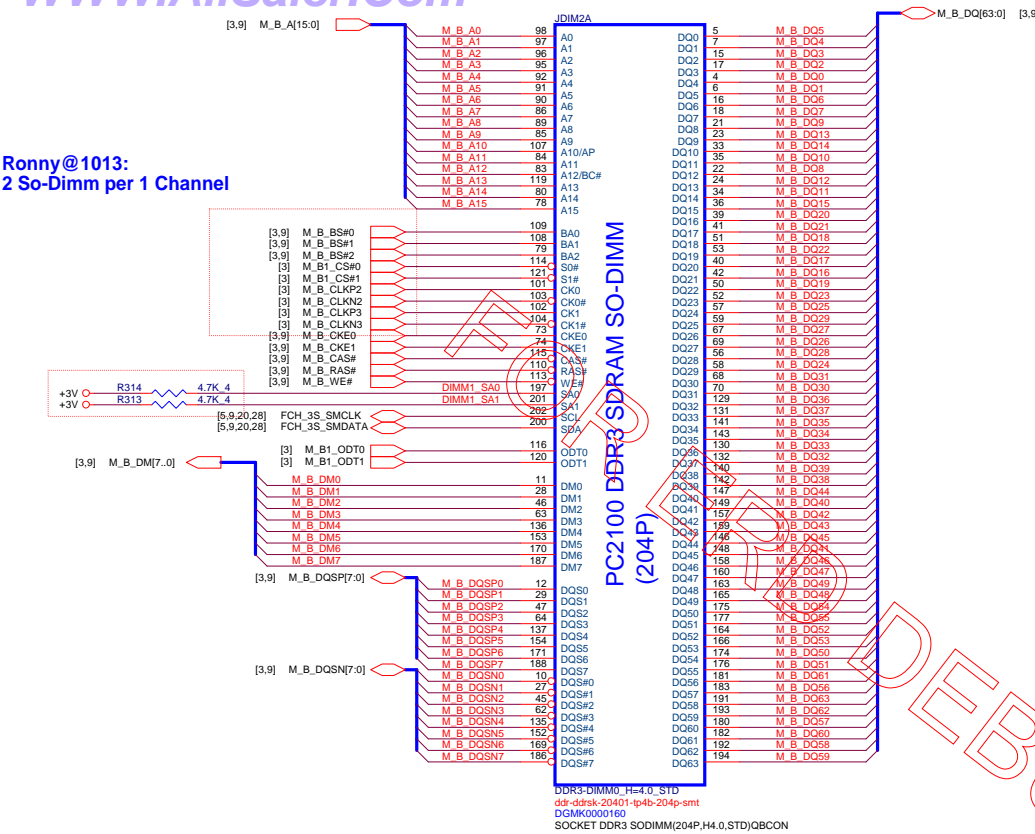
Size	Document Number	Rev
	Carrzio 7/7 (GND)	1A
Date: Friday, July 24, 2015	Sheet 8 of 62	

Ronny@1013:
2 So-Dimm per 1 Channel



PROJECT : 400 SERIES		
Quanta Computer Inc.		
Size	Document Number	Rev
Custom	System Memory 1/2 (4H)	1A
Date: Friday, July 24, 2015	Sheet 9 of 82	

Ronny@1013:
2 So-Dimm per 1 Channel



DDR3 Thermal Sensor

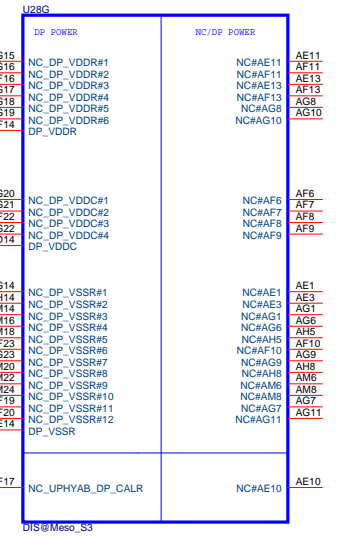
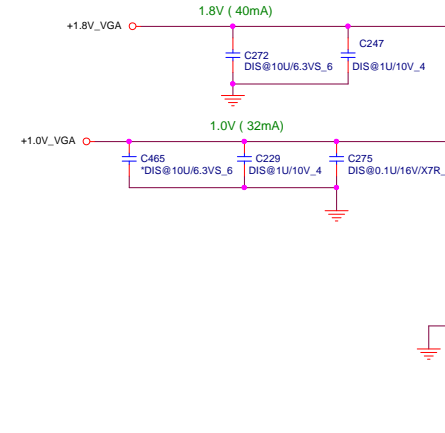
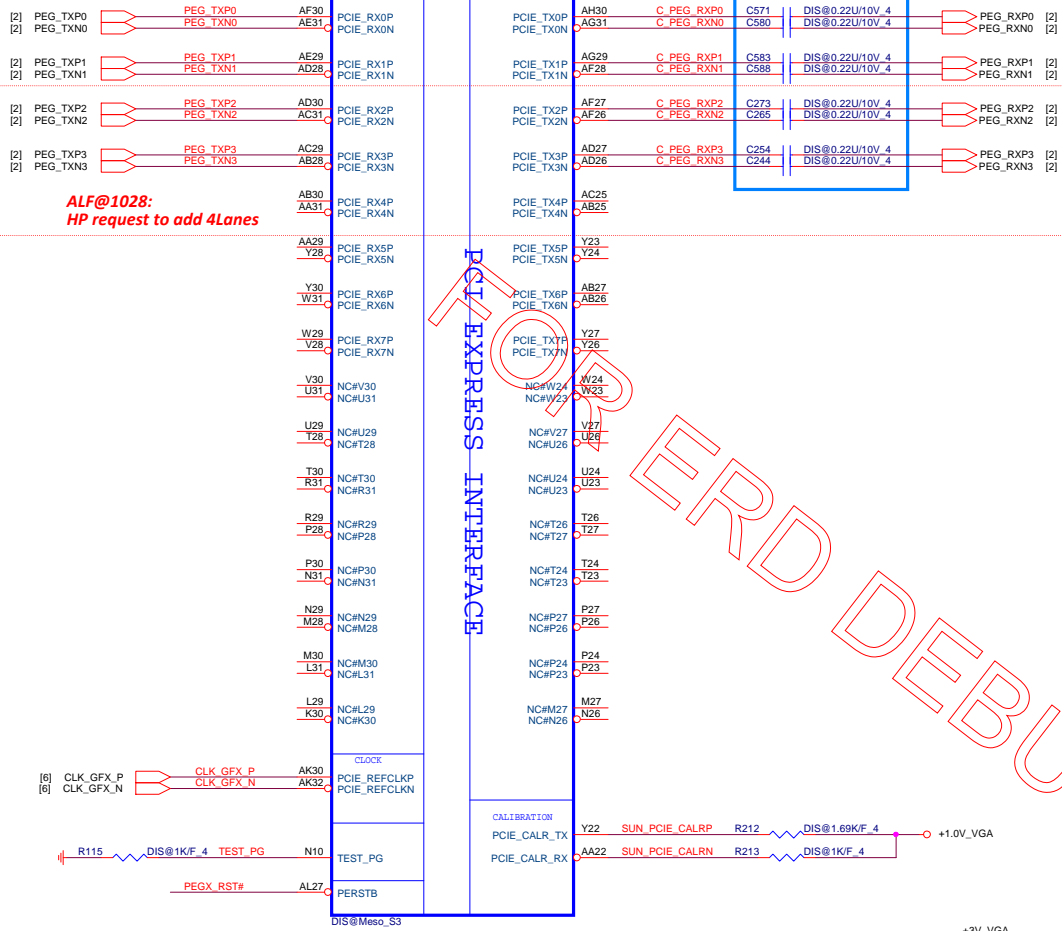
1028: Ronny
delete DDR thermal IC, please refer to Page41

PROJECT : 400 SERIES
Quanta Computer Inc.

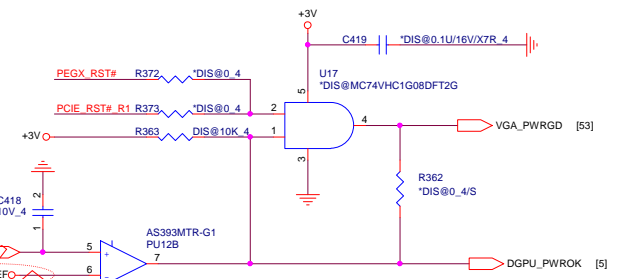
Size Custom	Document Number	Rev 1A
	System Memory 2/2 (4H)	
Date: Friday, July 24, 2015	Sheet 10 of 62	

Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4103K1B08

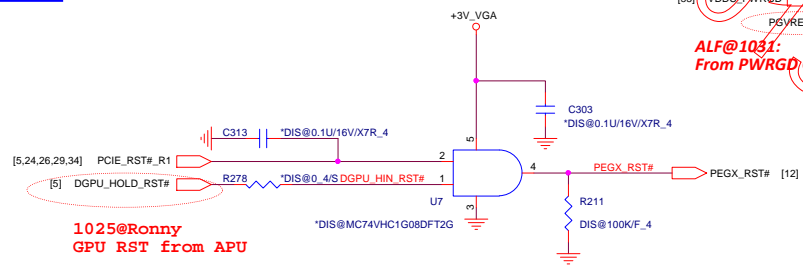
9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)



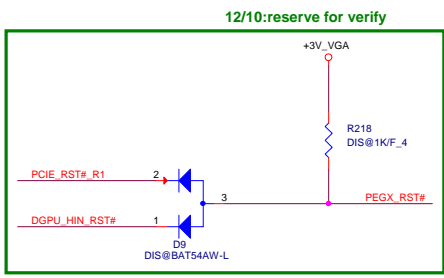
ALF@1031: Following the 2014 AMD Leading Schematic for DGPU_PWROK




ALF@1031: From PWRGD Generator



1025@Ronny GPU RST from APU



[12,14,53,55] +3V_VGA
[12,14,53,55] +1.8V_VGA
[14,55] +1.0V_VGA

 NB5	PROJECT : 400 SERIES Quanta Computer Inc.		
	Size	Document Number TOPAZ S3 PCIE/DP power	Rev 1/
Monday, July 28, 2015		Sheet 11 of 62	

10/2: remove TP for no use

9/11: follow CRB change to 10K

9/11: Add for SR Tool review result

AMD recommend

ALF@1029: Del GPU Thermal IC Circuit... and NC for those signals GPU_THERM1A GPU_THERM2C VGA_ALERT

10/1: Gen 3 support or not

BIT5 => BIT1

PS0 => 11001
PS1 => 11001
PS2 => 11000
PS3 => 11001

1108@RNY: AMD says reserved and non-stuff

Follow AMD check list

9/4: follow CRB design by FAE

MLPS Implementation

Connect GPD2_28 to 10K pull-down to enable MLPS.
If any of PS_0,1,2,3 not used, leave "no connect".
R, pu, R, pd and C must be properly populated per tables below.
Place MLPS circuit components as close to the ADC as possible.
Total DC resistance of trace between PS pin and C should be less than 2 ohms.
Total DC resistance of trace between C and ground should be less than 1 ohm.
Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance.

Capacitor Lookup Table		Resistor (Under Lookup Table)	
C (pF)	MLPS	R, pu (ohm)	R, pd (ohm)
680	00	NC	4750
82	01	8450	2000
10	10	4350	2000
NC	11	8880	4900
		4350	4900
		3240	5020
		3400	10000
		4750	NC

Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG(2:0)
128 MiB	000
256 MiB	001
512 MiB	010
Reserved	011
1 GiB	Not Supported
2 GiB	Not Supported
4 GiB	Not Supported

PS_3[3:1]	Vendor	Type	Vendor P/N	QCI P/N (BS/QCCOR)	PU	PD
000	Samsung- Q die	128Mx16 *4,1000MHz	K4W201646Q-BC1A	AKD5MG8T508/AKD5MG8T509	NC	4.75K
001	Samsung- E die	256Mx16 *4,1000MHz	K4W401646E-BC1A	AKD5PGD7500/AKD5PGD7501	8.45K	2K
010	Hynix- Huma F die	128Mx16 *4,1000MHz	H57C2633FF-11C	AKD5M2D7W02/AKD5M2D7W03	4.53K	2K
011	Hynix- C(Polaris)	256Mx16 *4,1000MHz	H57C4633CF-NC0C	AKD5PD2TW02/AKD5PD2TW03	5.98K	4.99K
100	Micron- K die	128Mx16 *4,1000MHz	MT41J128M163T-093G:K	AKD5MG8T116/AKD5MG8T117	4.53K	4.99K
101	Micron- S die	256Mx16 *4,1000MHz	MT41J256M16A-093G:E	AKD5P2ST100/AKD5P2ST101	3.24K	5.62K
110	Nanya- F die	128Mx16 *4,1000MHz	NT5CB128M16FP-FL	AKD5MG8T700/AKD5MG8T701	3.4K	10K
111	Nanya- D die	256Mx16 *4,1000MHz	NT5CB256M16DP-FL	AKD5PGD7F02/AKD5PGD7F03	4.75K	NC

Vendor ID

00 = Samsung
01 = Hynix
10 = Micron
11 = Nanya

VRAM density

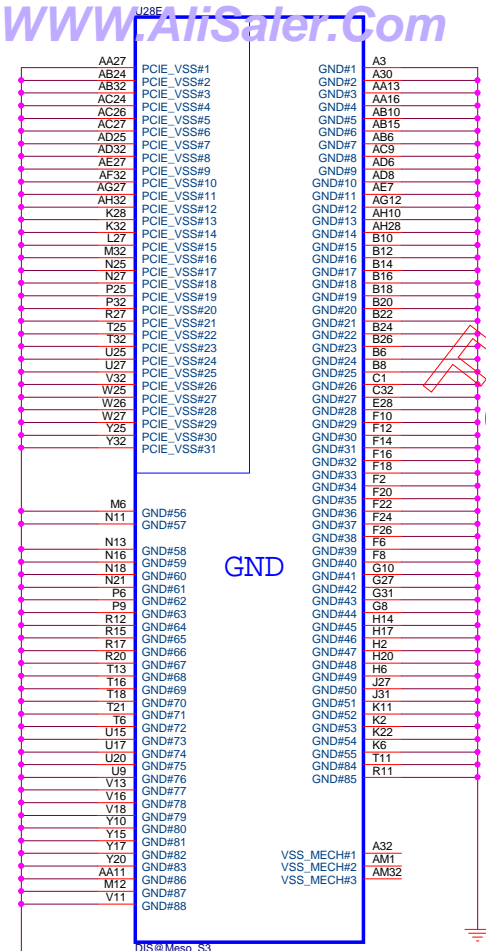
0=128Mx16
1=256Mx16

Memo Multi-level Pin Straps

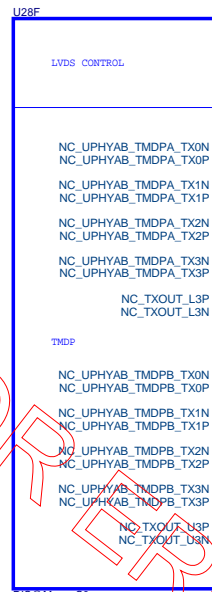
MLPS Bit: PS_3 mapping between the bit values and resistor values

PROJECT : 400 SERIES
Quanta Computer Inc.

Size: **TOPAZ_S3_Main**
Date: **Fri, 24 Jul 2015**



U28F



DIS@ Meso_S3

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

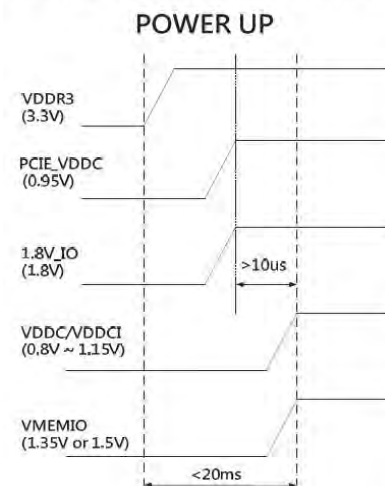
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYN	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

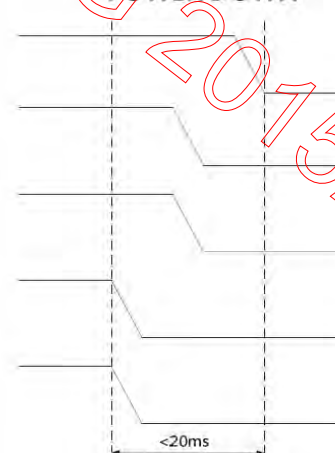
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

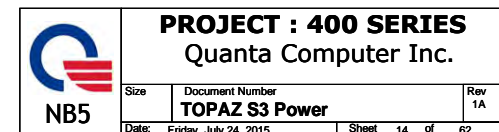


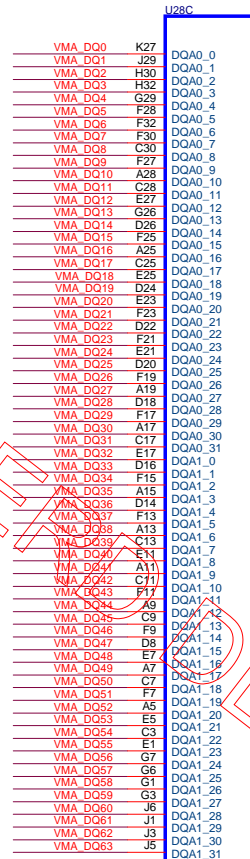
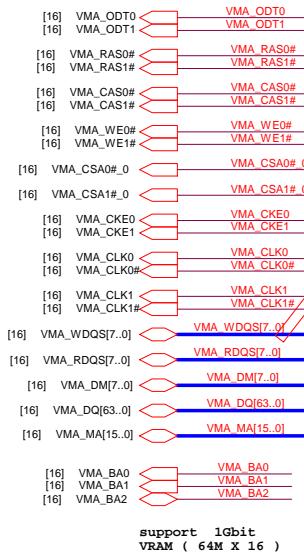
POWER DOWN



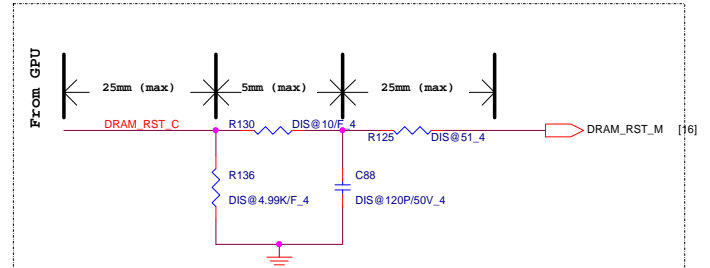
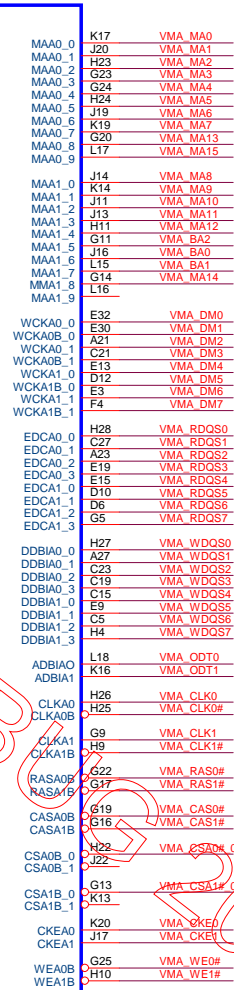
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A
Date:	Friday, July 24, 2015	Sheet 13 of 62



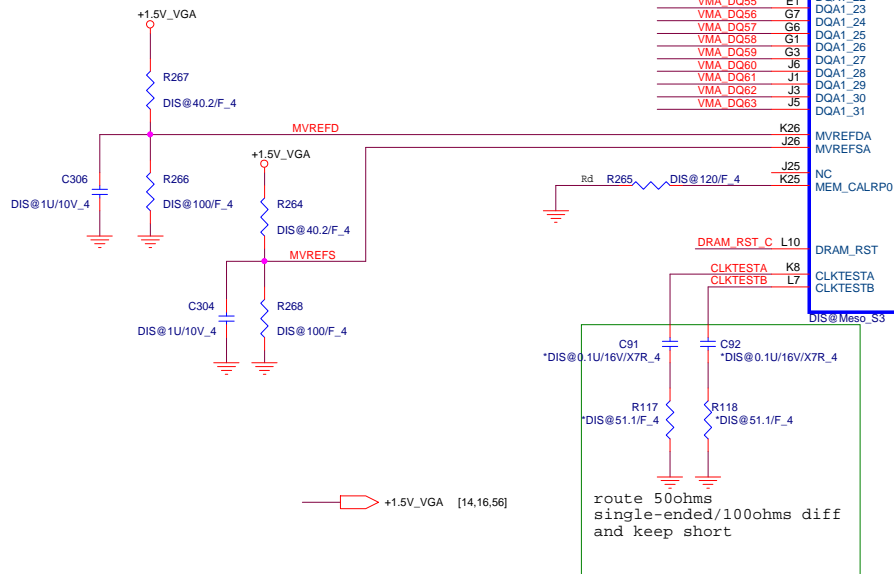


MEMORY INTERFACE

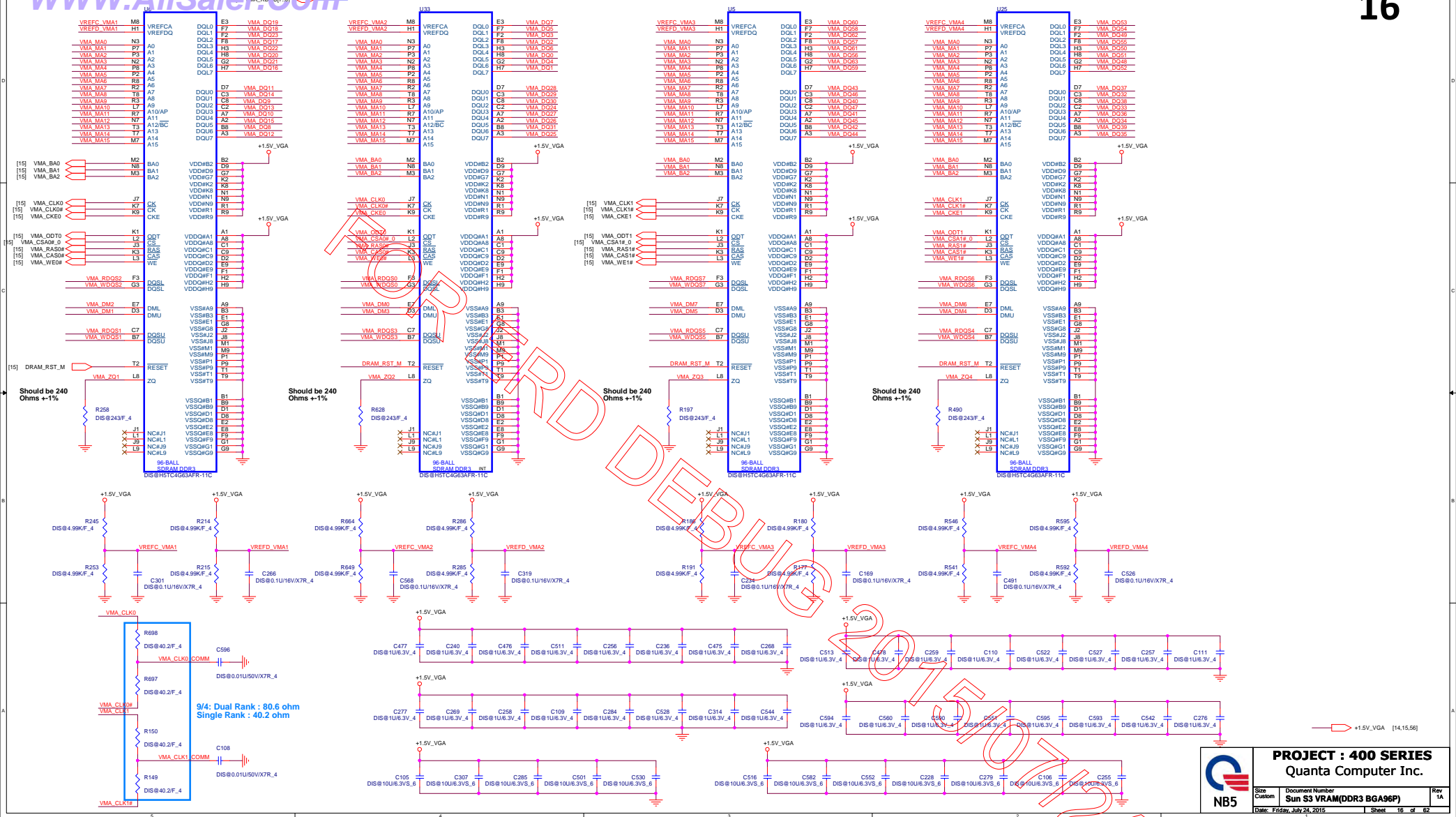


Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

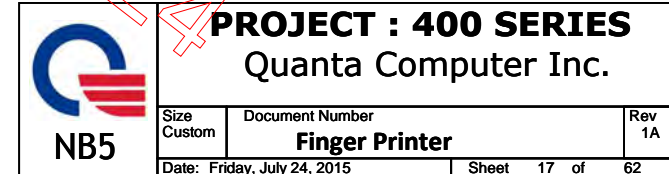
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.



NB5	PROJECT : 400 SERIES Quanta Computer Inc.		
	Size	Document Number	Rev 1A
		TP0AZ_S3_MEM_Interface	
	Date: Friday, July 24, 2015	Sheet 15 of 62	



Fingerprint Conn



400 series O330 Delete DP DemultiPlexer due to not support docking

400 series 1001 change to LVDS/eDP co-design


ALF@1119:
HP confirmed to remove the eDP to LVDS convertor.

FOR ERD DEBUG 2015/07/24

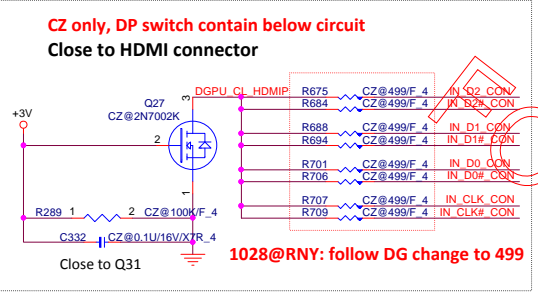
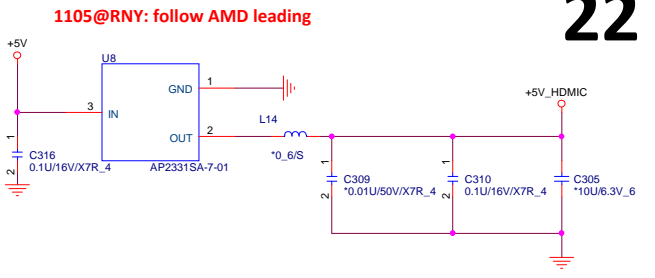
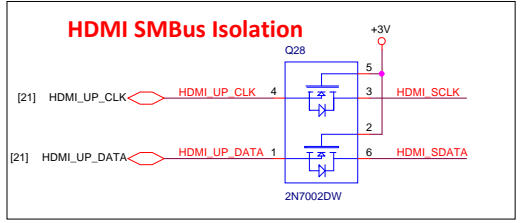
[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,52,58]

+3V



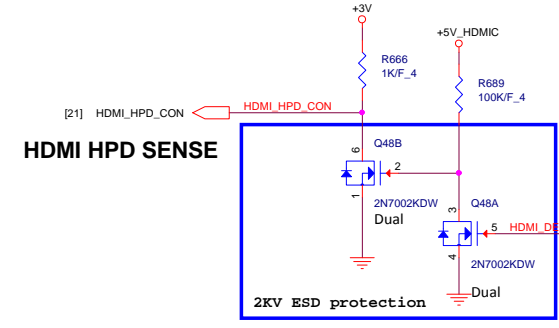
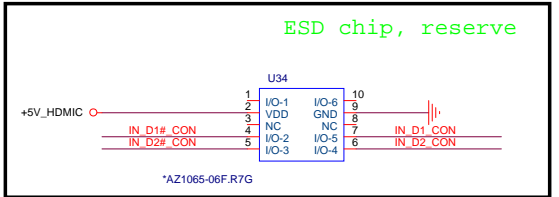
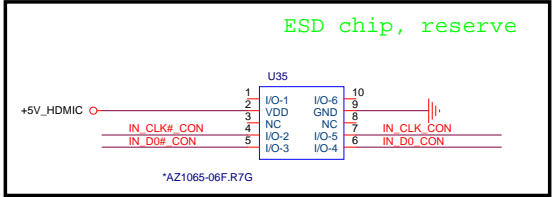
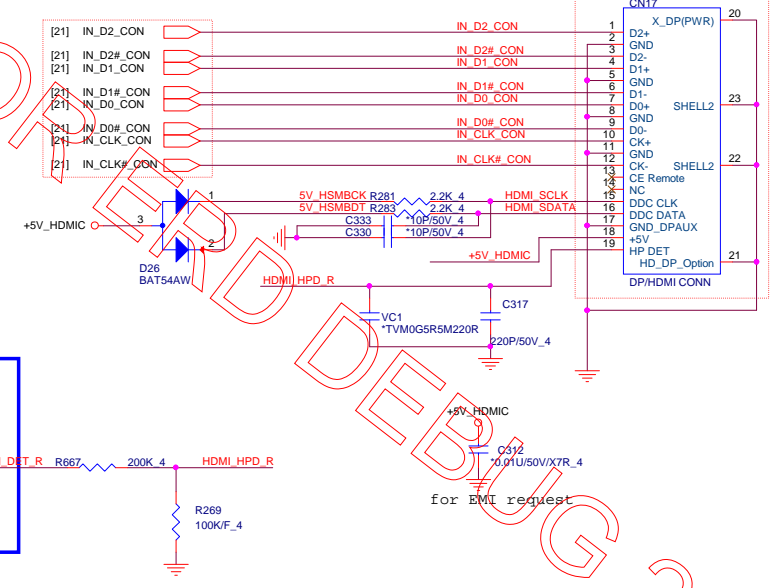
 NB5	PROJECT : 400 SERIES Quanta Computer Inc.		
	Size Custom	Document Number RTD2136	Rev 1A
	Date: Friday, July 24, 2015	Sheet 18	of 62





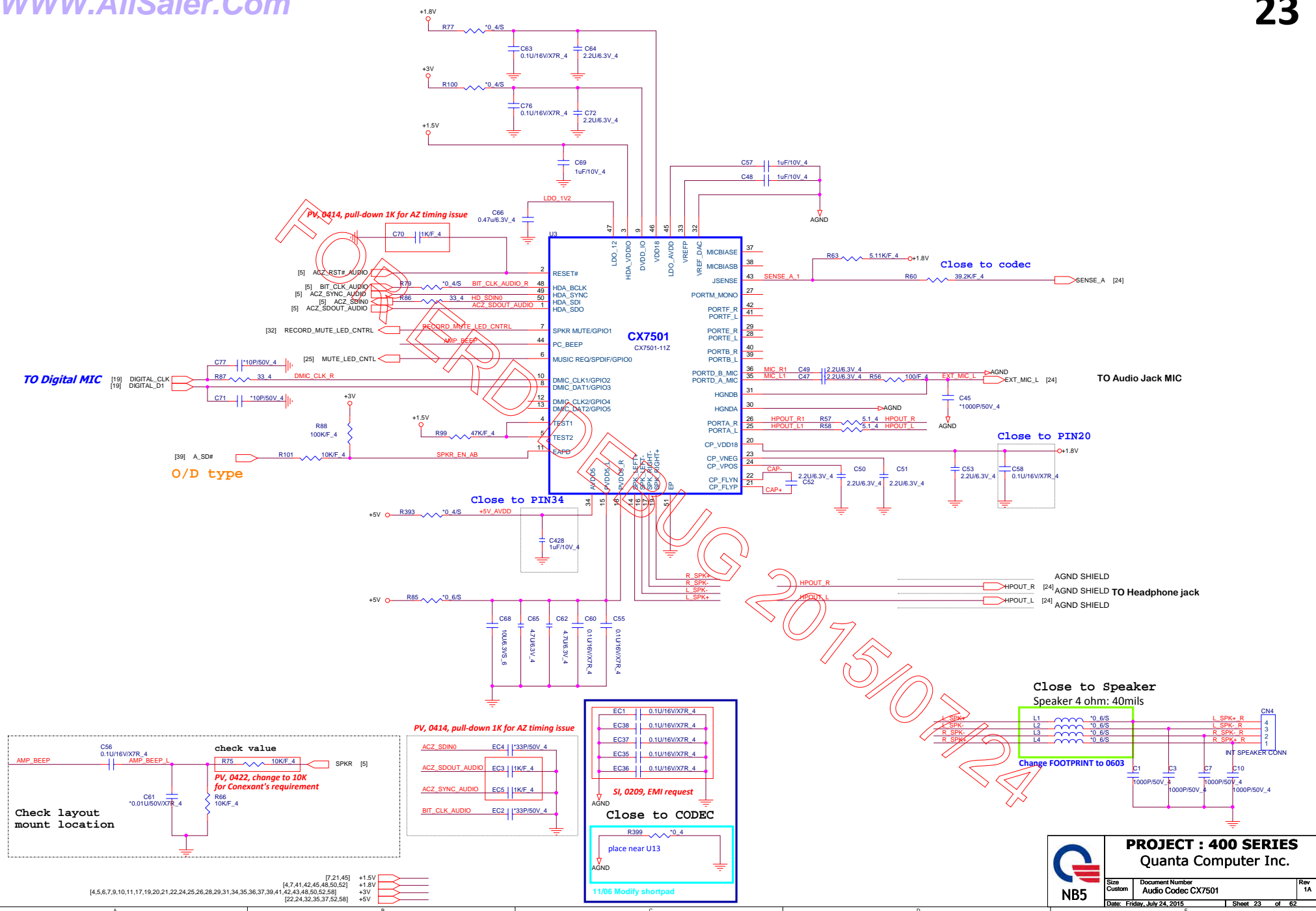
1014@Ronny : remove re-driver IC
1015@Ronny: Add DP Switch
1016@Alfred: Changed the DDI1 to DDI2

1028@Ronny : change FP only
need confirm PN then change PN



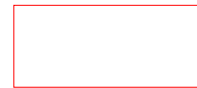
1028@RNY: follow X21 HPD circuit

for EMI request

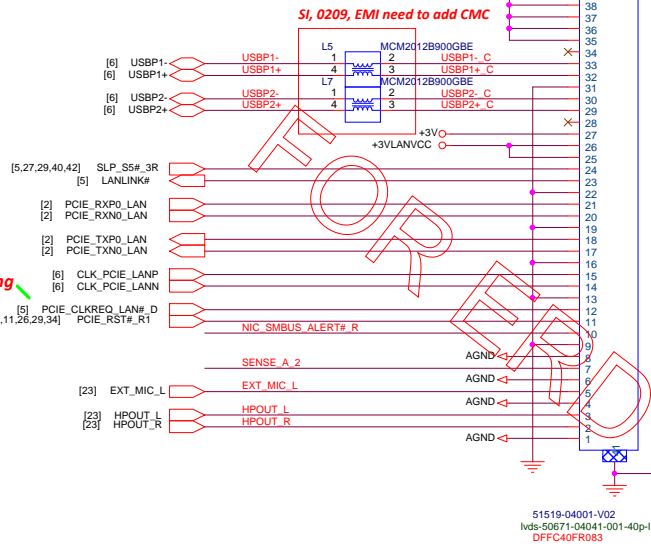
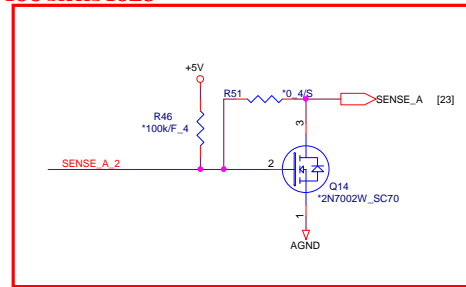


USB2.0 x2/LAN/Headphone_Mic Combo Jack Daughter Board Connector

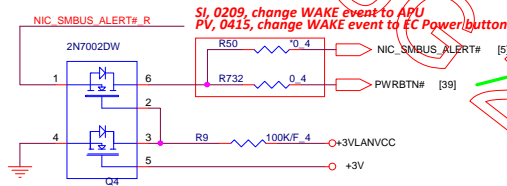
PVR, 0720, delete USB 0 ohm co-lay



400 series 1029



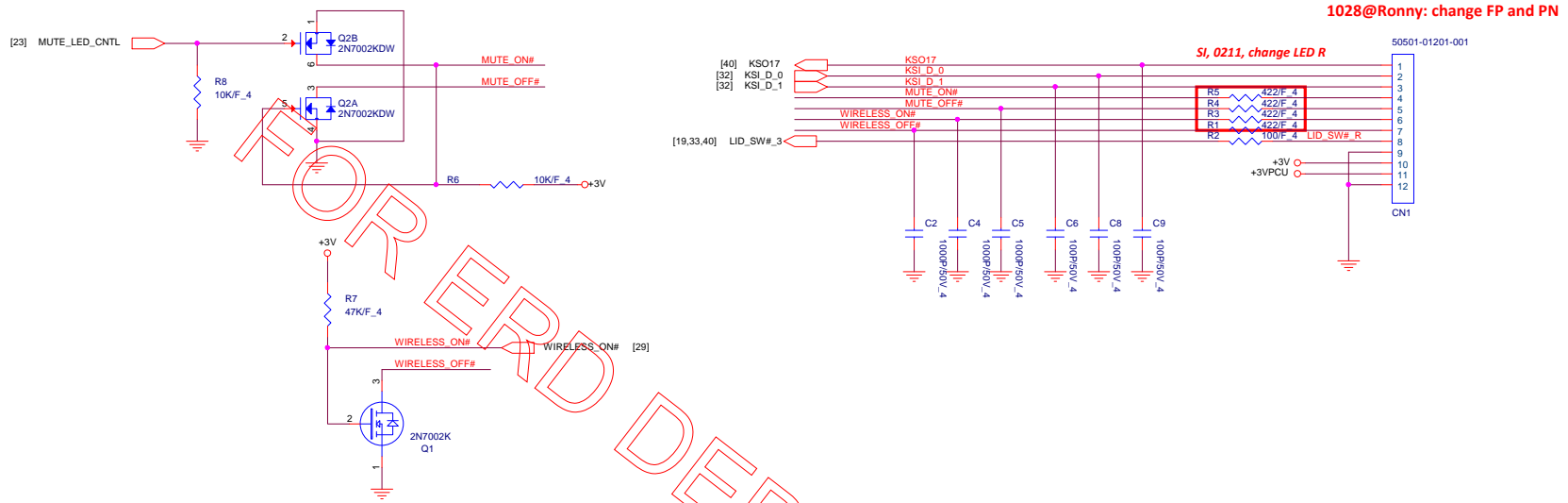
ALF@1025:
Following AMD Leading




ALF@1031:
HP requested LAN PCIE wake to PWRBTN#

ALF@1031:
Needs to add 1 Pin for LAN Link to FCH.
Waiting for discussing with internal team

		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size	Custom	Document Number	Rev
		Audio/USB BOARD	1A
Date: Friday, July 24, 2015		Sheet 24 of 62	



 PROJECT : 400 SERIES Quanta Computer Inc.		Rev 1A
		Size Custom
Document Number Function Conn./LED		
Date: Friday, July 24, 2015		Sheet 25 of 62

1023@Ronny: follow Leading platform

ALF@1106:
When CZ, Stuff Q1

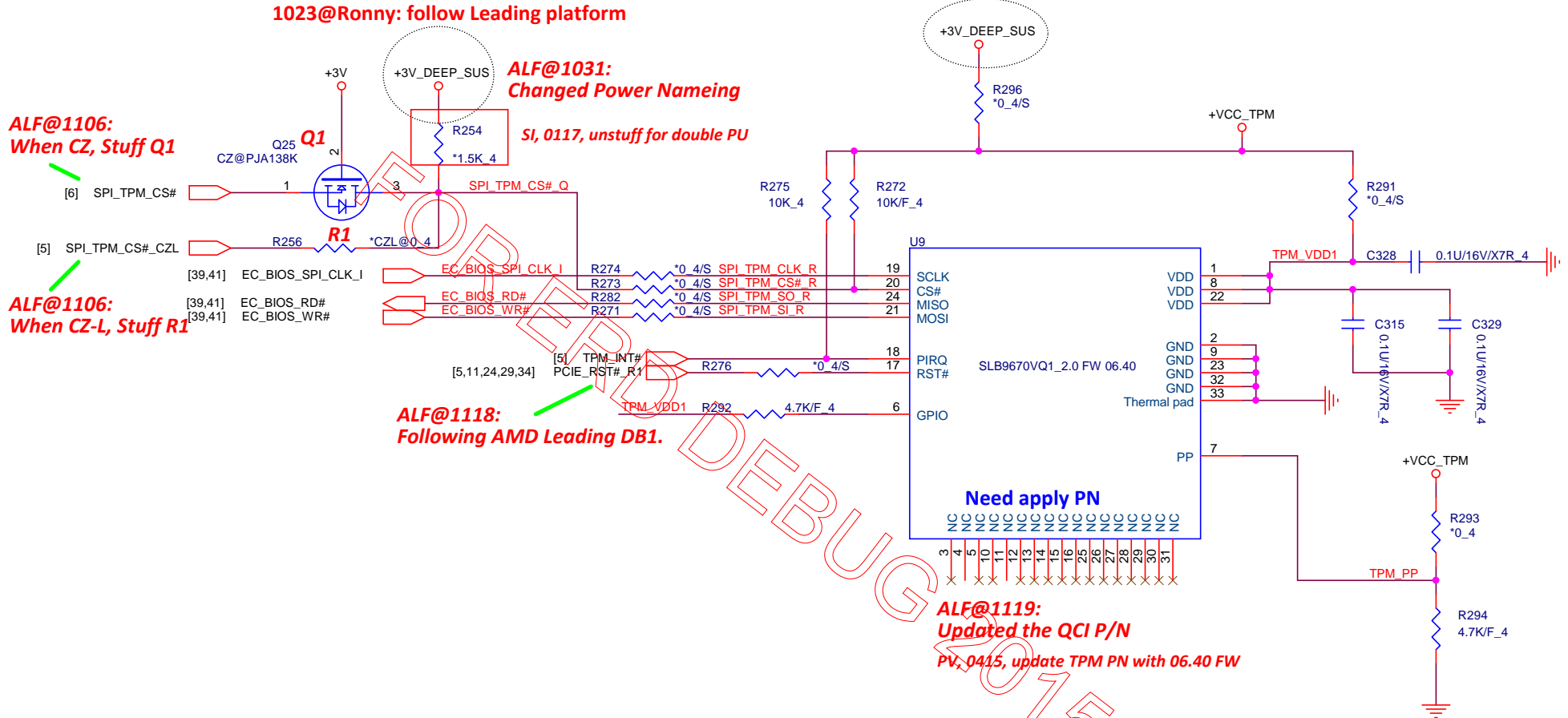
ALF@1106:
When CZ-L, Stuff R1

ALF@1031:
Changed Power Nameing

SI, 0117, unstuff for double PU

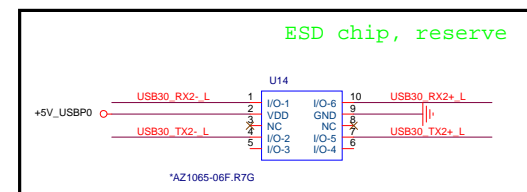
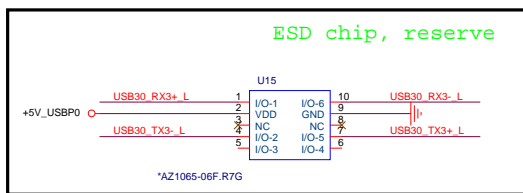
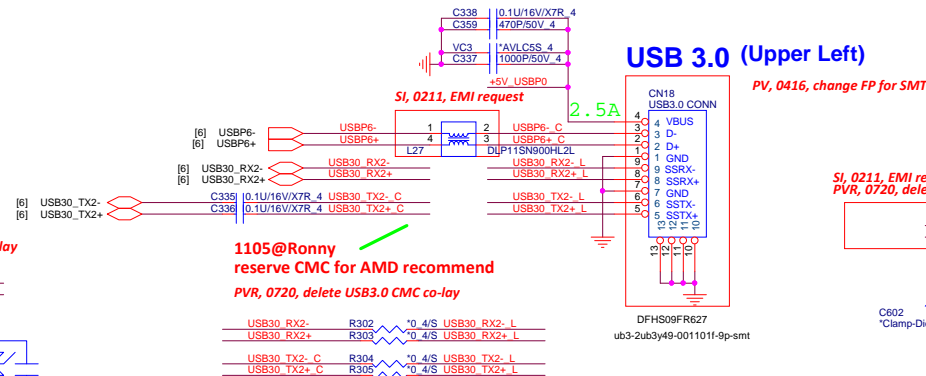
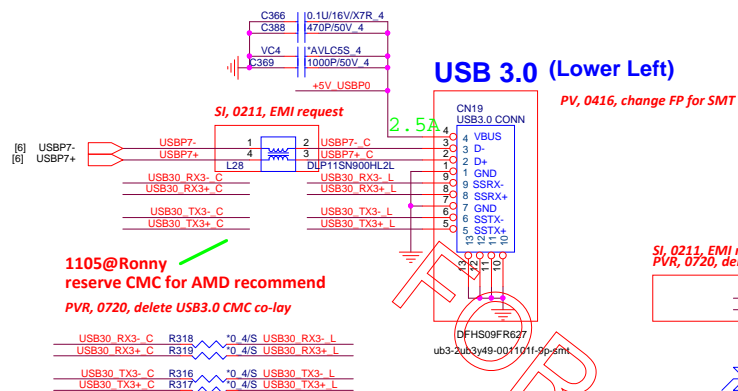
ALF@1118:
Following AMD Leading DB1.

ALF@1119:
Updated the QCI P/N
PV, 0415, update TPM PN with 06.40 FW



PROJECT : 400 SERIES
Quanta Computer Inc.

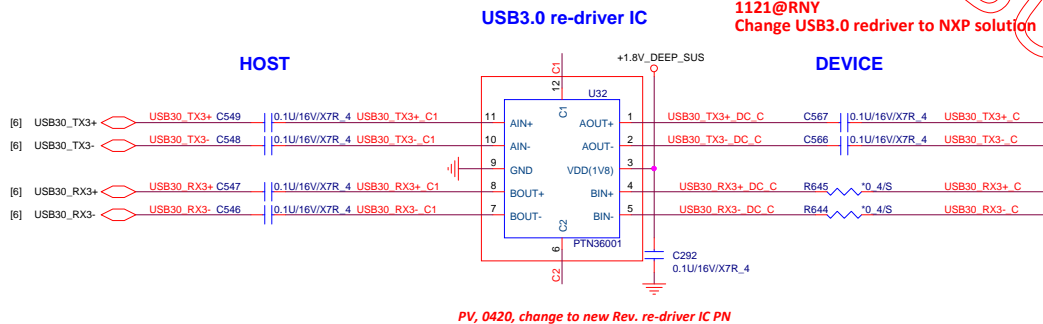
Size Custom	Document Number TPM SLB9665_QFN	Rev 1A
Date: Friday, July 24, 2015	Sheet 26 of 62	



USB3.0

USB3.0 Re-driver IC

1016: Alfred
Added USB3.0 Re-driver for Lower Left.



1112@ALF
Deleted the bypass way, due to the space limitation.

USB3.0 bypass 0 ohm

Layout Notes:
Stubs Trace less than 150mil

1108@RNY
Change to Active High part

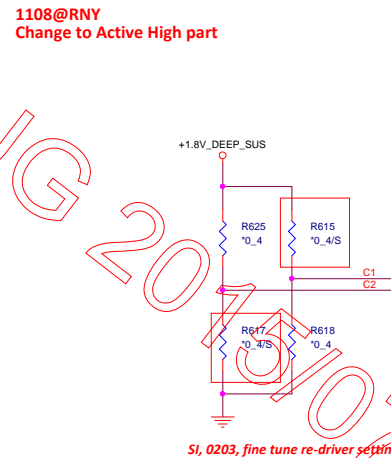


Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[2]	DE[2]	OS[2]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[1]	OS[1]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V



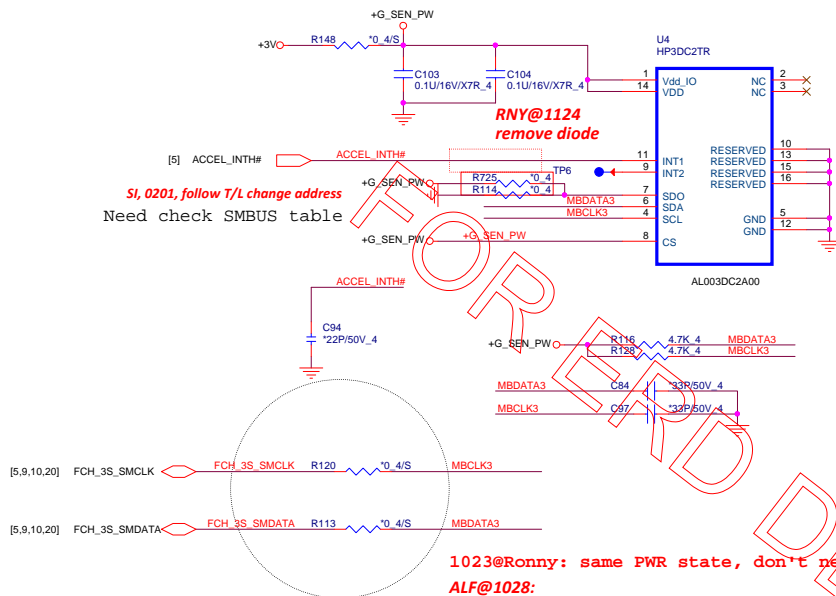
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB 3.0/USB3 Re-driver	1A
Date: Friday, July 24, 2015	Sheet 27 of 62	

400 series (920) Delete USB 3.0 redriver due to not support docking

Accelerometer Sensor

G-Sensor Power need check



Touch screen


ALF@1028:
HP Confirmed, 400 Series AMD does NOT support the Touch Screen.

1028@Ronny:
need change pin define

[24,27,31,34,43,44,45,46,47,48,50,52,53,55,56,58] +5VPCU
[7,29,32,33,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

		PROJECT : 400 SERIES Quanta Computer Inc.	
Size Custom	Document Number Accelerometer	Rev 1A	
Date: Friday, July 24, 2015	Sheet 28 of 62		




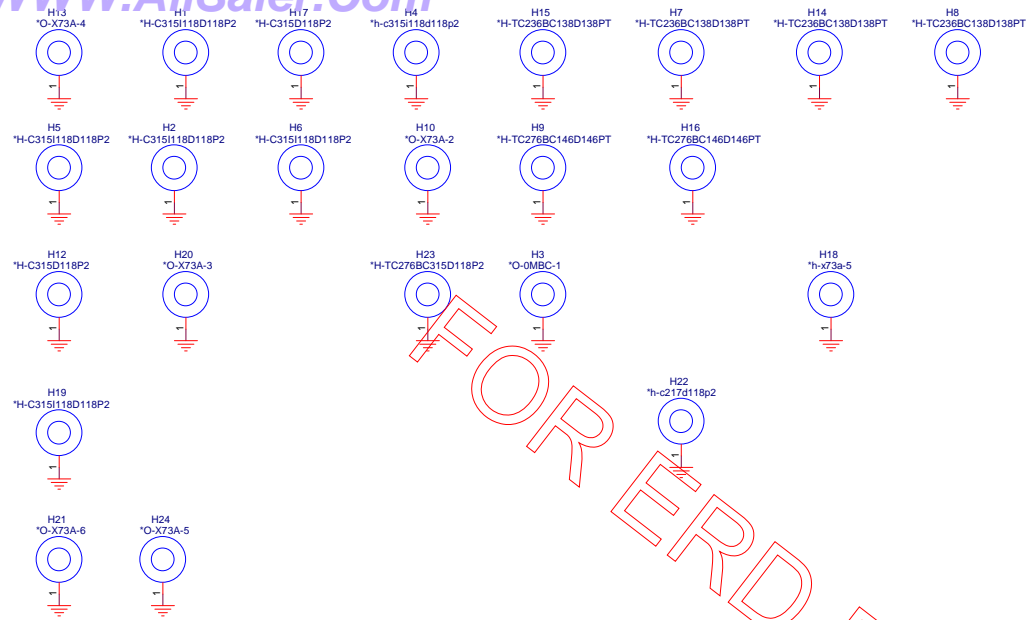
 NB5	PROJECT : 400 SERIES Quanta Computer Inc.		
	Size Custom	Document Number NGFF WLAN/BT	Rev 1A
Date: Monday, July 27, 2015		Sheet 29 of 62	

ALF @ 02 :
400 Series AMD does Not support the WWAN.
So, Del the related WWAN_DET# components.

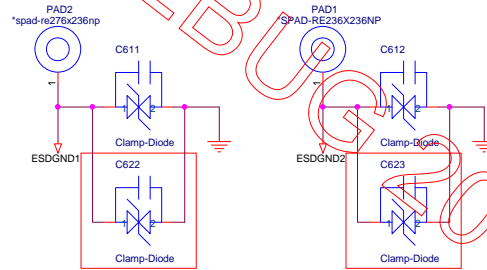
RNY@1209:
400 Series AMD does Not support the M.2 SSD

FOR ERD DEBUG 2015/07/24

 NB5		PROJECT : 400 SERIES Quanta Computer Inc.	
		Size Custom Document Number WWAN NGFF or SSD Date: Friday, July 24, 2015	Rev 1A Sheet 30 of 62

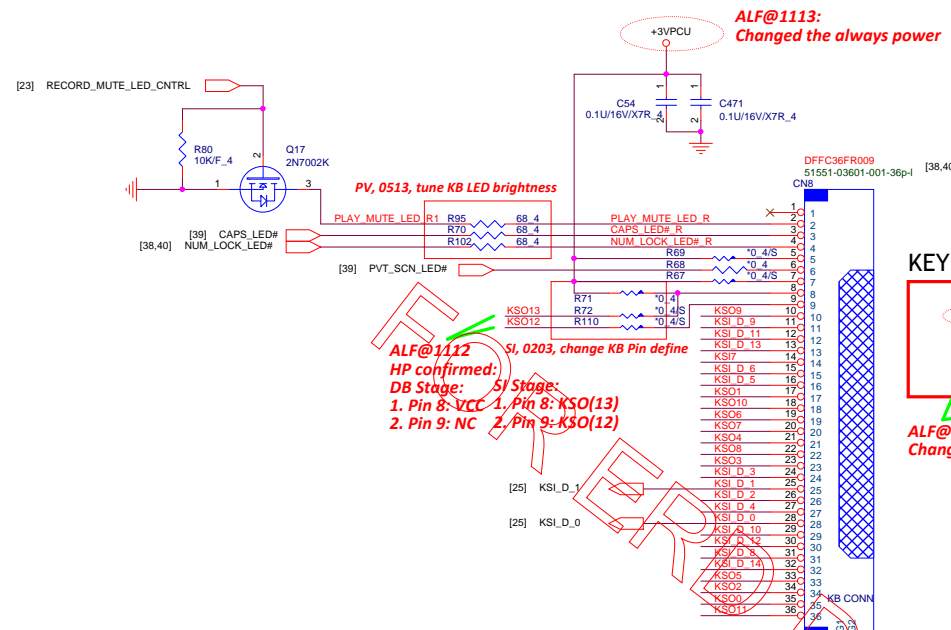


EMI CAP

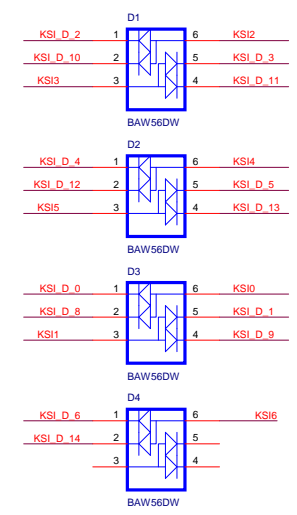
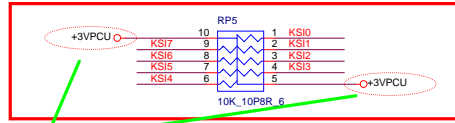


PV_0422, reserve one more ESD part at each ESDGND
PV_0514, stuff varistor

	PROJECT : 400 SERIES		
	Quanta Computer Inc.		
	Size Custom	Document Number HOLE	Rev 1A
	Date: Friday, July 24, 2015	Sheet 31	of 62



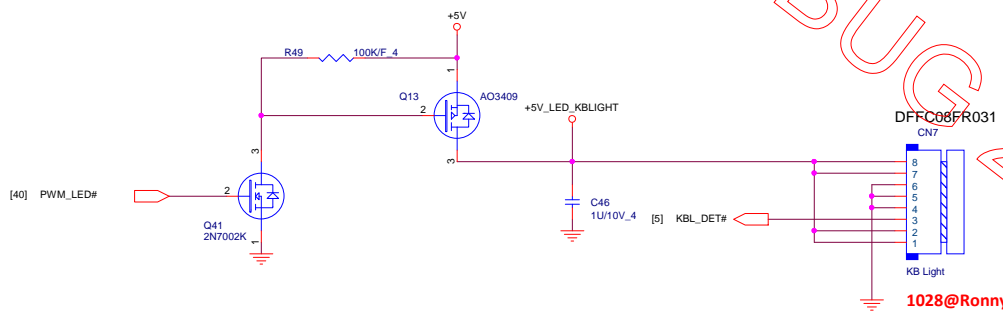
KEYBOARD PULL-UP



*100pF 2	C469	KSO9
*100pF 2	C89	KSI_D_9
*100pF 2	C96	KSI_D_11
*100pF 2	C99	KSI_D_13
*100pF 2	C101	KSI7
*100pF 2	C102	KSI_D_6
*100pF 2	C107	KSI_D_5
*100pF 2	C115	KSO1

*100pF 2	C124	KSO10
*100pF 2	C130	KSO6
*100pF 2	C138	KSO7
*100pF 2	C145	KSO4
*100pF 2	C153	KSO8
*100pF 2	C155	KSO3
*100pF 2	C165	KSI_D_3
*100pF 2	C181	KSI_D_1

*100pF 2	C190	KSI_D_2
*100pF 2	C196	KSI_D_4
*100pF 2	C210	KSI_D_0
*100pF 2	C221	KSI_D_10
*100pF 2	C225	KSI_D_12
*100pF 2	C515	KSI_D_8
*100pF 2	C521	KSI_D_14
*100pF 2	C523	KSO5



[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,52,58] +3V
[22,23,24,35,37,52,58] +5V
[7,25,33,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

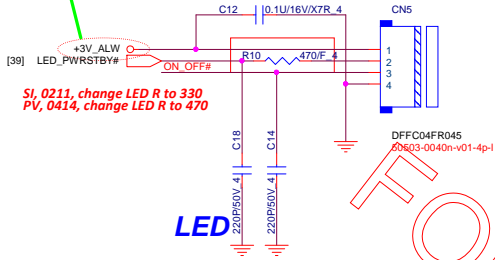
PROJECT : 400 SERIES
Quanta Computer Inc.

Size Custom	Document Number KB/KB light	Rev 1A
Date: Friday, July 24, 2015	Sheet 32 of 62	

Power Botton Connector

1112@RNY: change to 4Pin FP and PN

ALF@1115:
HP requested to modify the Power Switch.




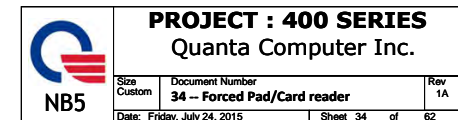
SI, 0211, change LED R to 330
PV, 0414, change LED R to 470

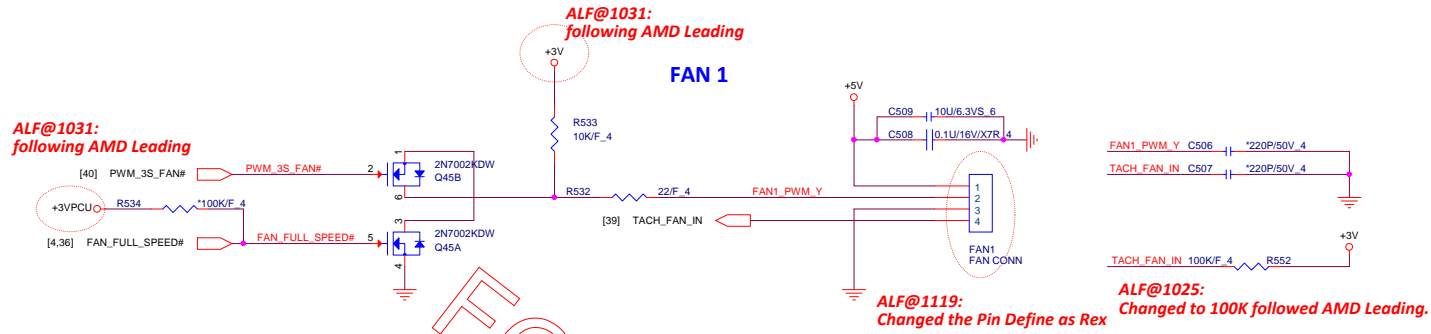
ALF@1114:
HP requested to reserve the reset IC

ALF@1119:
Updated the QCI P/N


[42,43,44,57] +3V_ALW
[45,6,7,9,10,11,17,18,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,52,58] +3V
[22,23,24,32,35,37,52,58] +5V
[7,25,32,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

		PROJECT : 400 SERIES Quanta Computer Inc.	
Size Custom	Document Number 33 -- PB/LID	Rev 1A	
Date: Friday, July 24, 2015	Sheet 33 of 62		



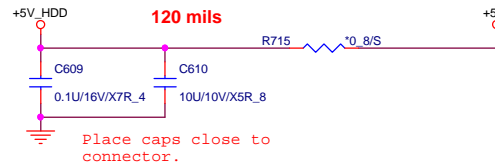
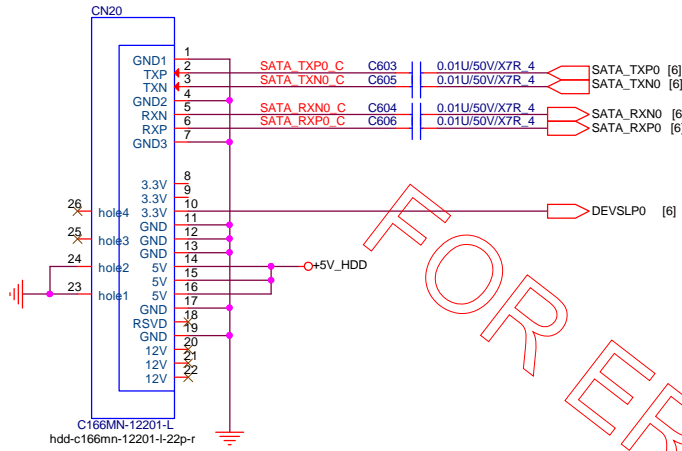


[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,36,37,39,41,42,43,48,50,52,58] +3V
 [22,23,24,32,37,52,58] +5V
 [7,25,32,33,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU
 [24,27,31,34,43,44,45,46,47,48,50,52,53,55,56,58] +5VPCU

		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size Custom	Document Number 35 -- FAN	Rev 1A	
Date: Friday, July 24, 2015		Sheet 35 of 62	

SATA-HDD

400 series 0929 Footprint and P/N TBD



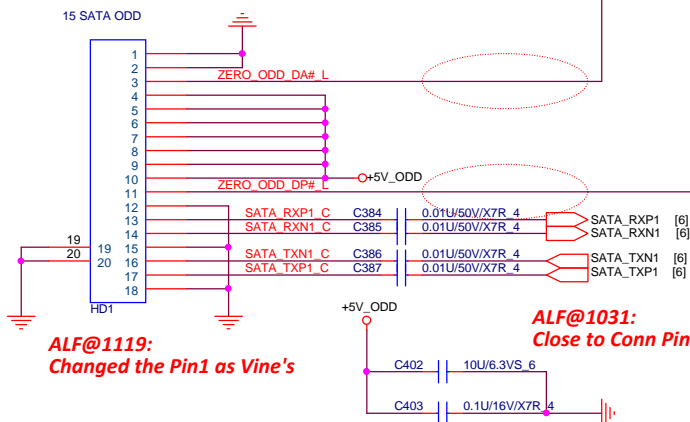
1028@Ronny: change to Vine 15" CONN

SATA-ODD

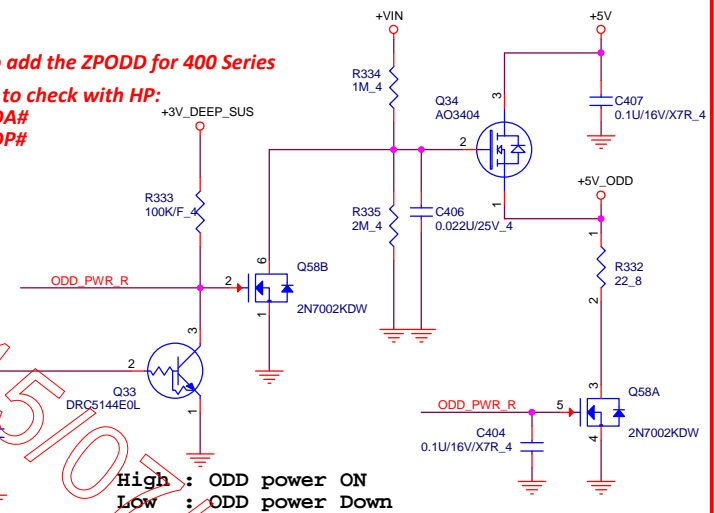
ALF@1031:
HP requested to add the ZPODD for 400 Series

GPIO PIN needs to check with HP:

1. ZERO_ODD_DA#
2. ZERO_ODD_DP#
3. ODD_PWR



ALF@1031:
Close to Conn Pin



[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,39,41,42,43,48,50,52,58]
[22,23,24,32,35,52,58]
[7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,52,55,57]

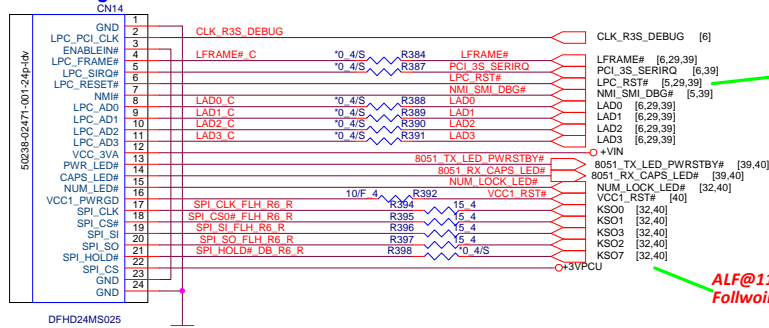
+3V
+5V
+3VPCU



PROJECT : 400 SERIES
Quanta Computer Inc.

Size B	Document Number 37 -- HDD/ODD	Rev 1A
Date: Friday, July 24, 2015	Sheet 37 of 62	


EC debug conn.



ALF@1027:
Following AMD Leading.

ALF@1115:
Following it in AMD Leading DB1.

1028@Ronny: change PN to DFHD24MS025

 PROJECT : 400 SERIES Quanta Computer Inc.		Size	Document Number	Rev
		Custom	38 - EC debug conn	1A
Date: Friday, July 24, 2015		Sheet 38 of 62		

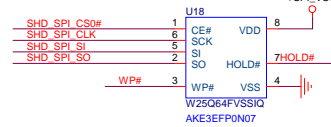




APU SPI ROM

Vender	Size	P/N (3.3V)	
WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
GGD	8M	AKE2EZN0Q00	GD25B64CSIGR
Socket			DG008000004

U18&U19 footprint 要重疊

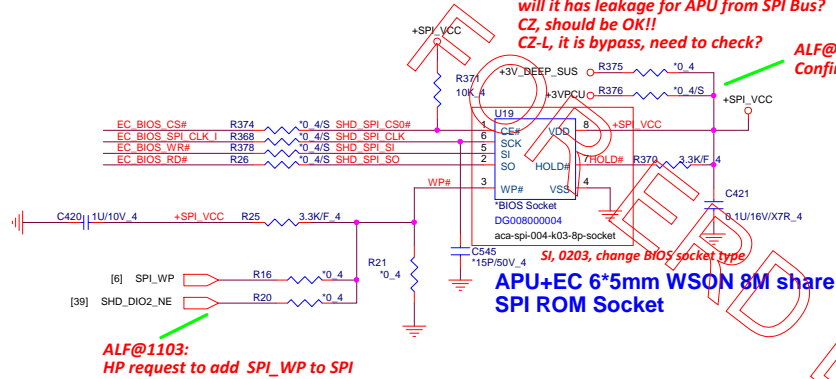


ALF@1031:
Needs to confirm EC Vendor, if use +3VPCU,
will it has leakage for APU from SPI Bus?
CZ, should be OK!!
CZ-L, it is bypass, need to check?

ALF@1113:
Confirmed HP, SPI Power Rail same as EC.

Alfred@1015:
Add flash ROM for first bring up (2MB ROM)
EC 6*5mm WSON 8M
SPI ROM Socket

SI, 0203, remove EC debug ROM



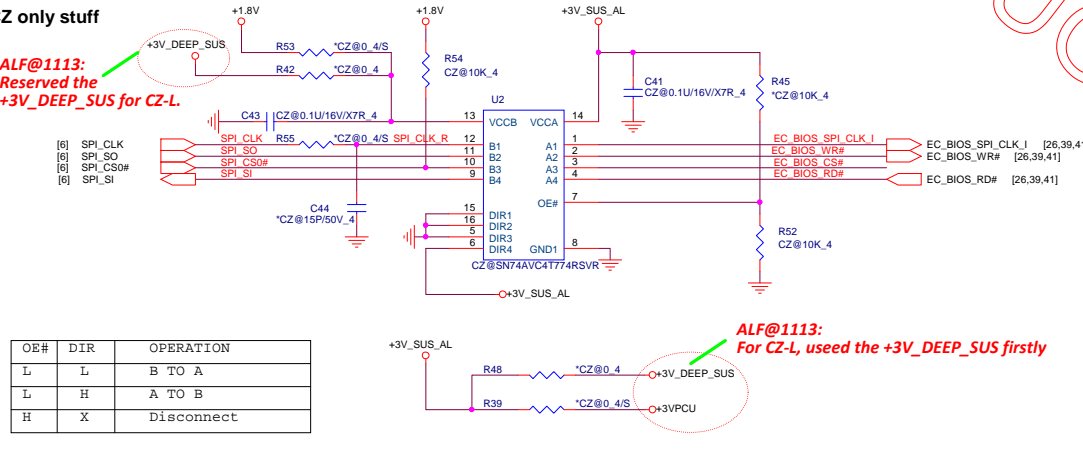
APU+EC 6*5mm WSON 8M share
SPI ROM Socket

From EC



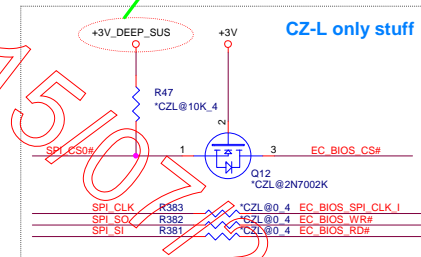
CZ only stuff

ALF@1113:
Reserved the
+3V_DEEP_SUS for CZ-L.



ALF@1113:
For CZ-L, used the +3V_DEEP_SUS firstly

ALF@1113:
1. SPI bus isolation to FCH



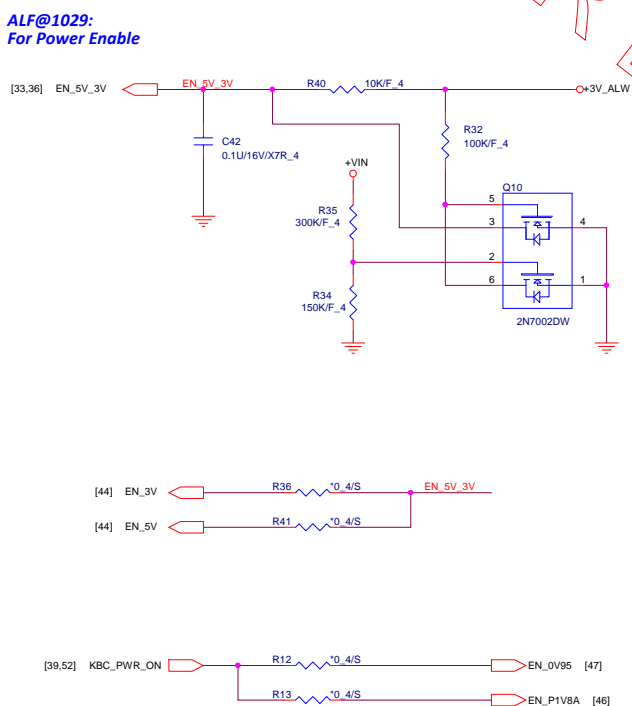
OE#	DIR	OPERATION
L	L	B TO A
L	H	A TO B
H	X	Disconnect

PROJECT : 400 SERIES
Quanta Computer Inc.

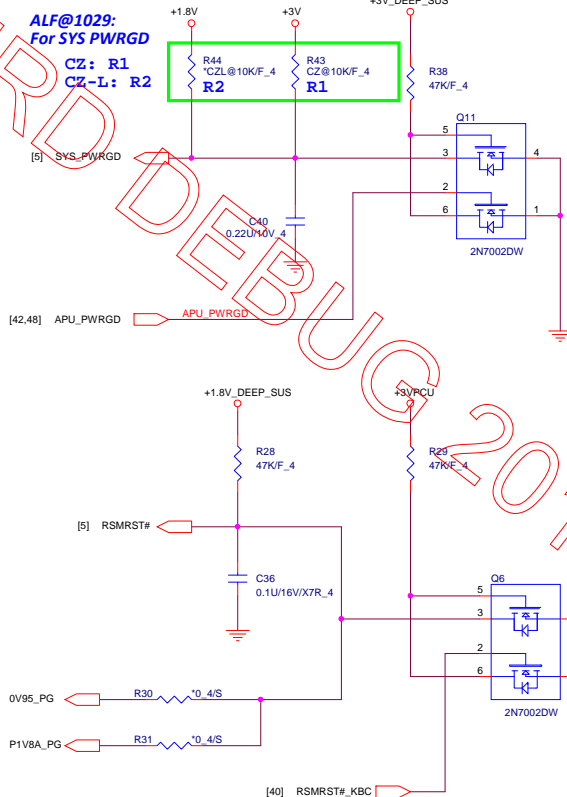
Size Custom	Document Number Flash(KBC+PCH)	Rev 1A
Date: Friday, July 24, 2015	Sheet 41 of 62	

ALF@1114:
Deleted the circuit of PWROK Generate followed T/L Leading.

ALF@1029:
For Power Enable



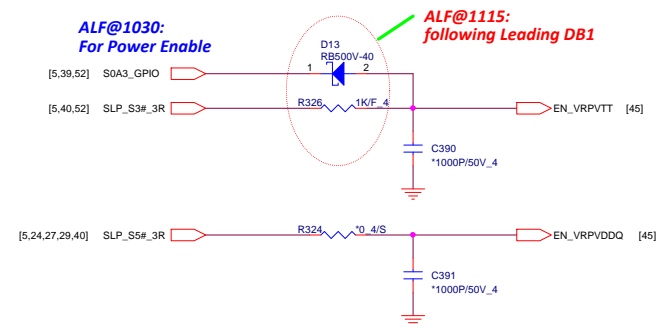
ALF@1029:
For SYS PWROK




ALF@1030:
For System PG

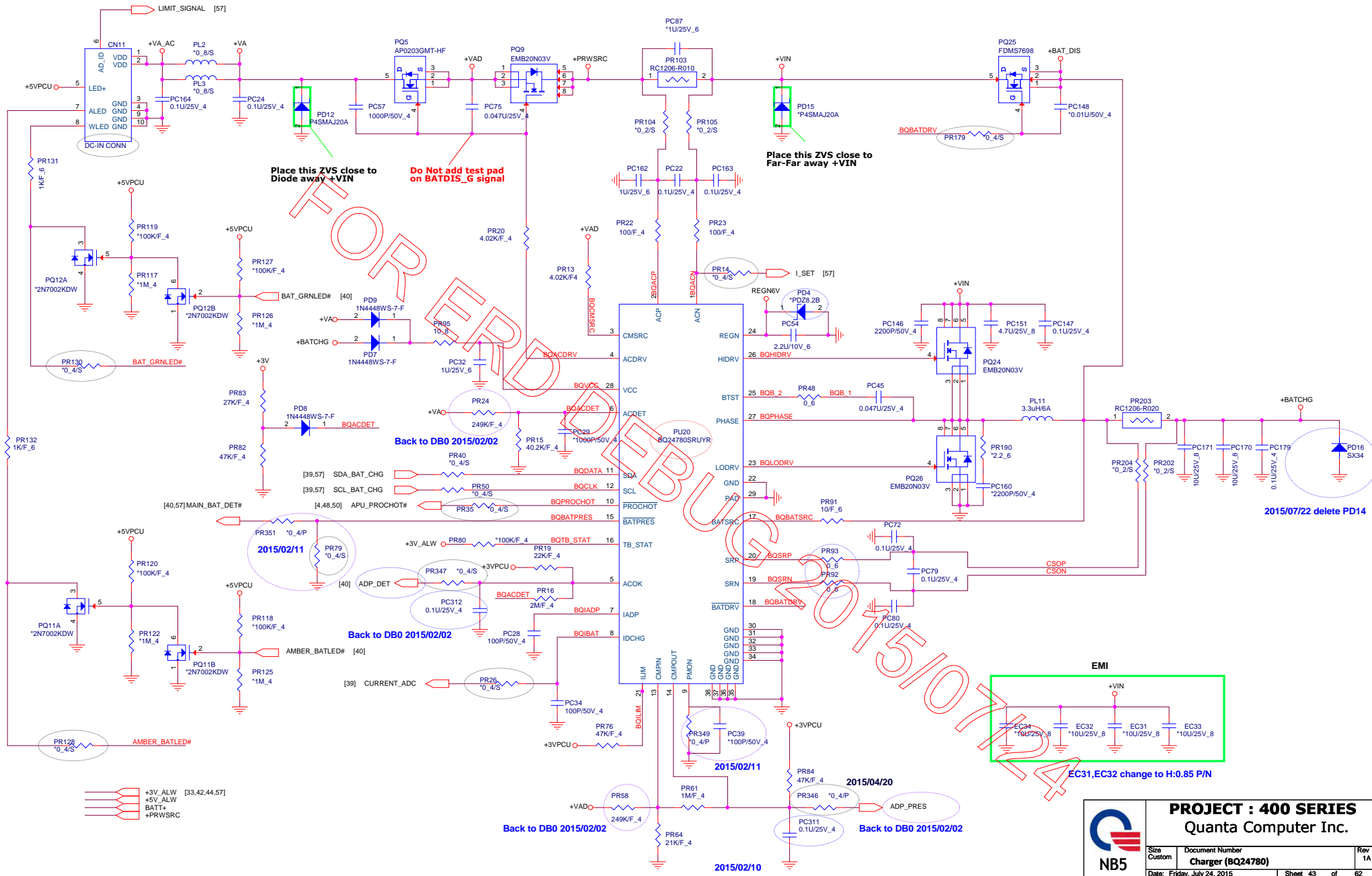


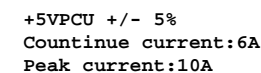
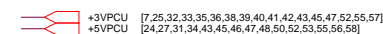
ALF@1030:
For Power Enable



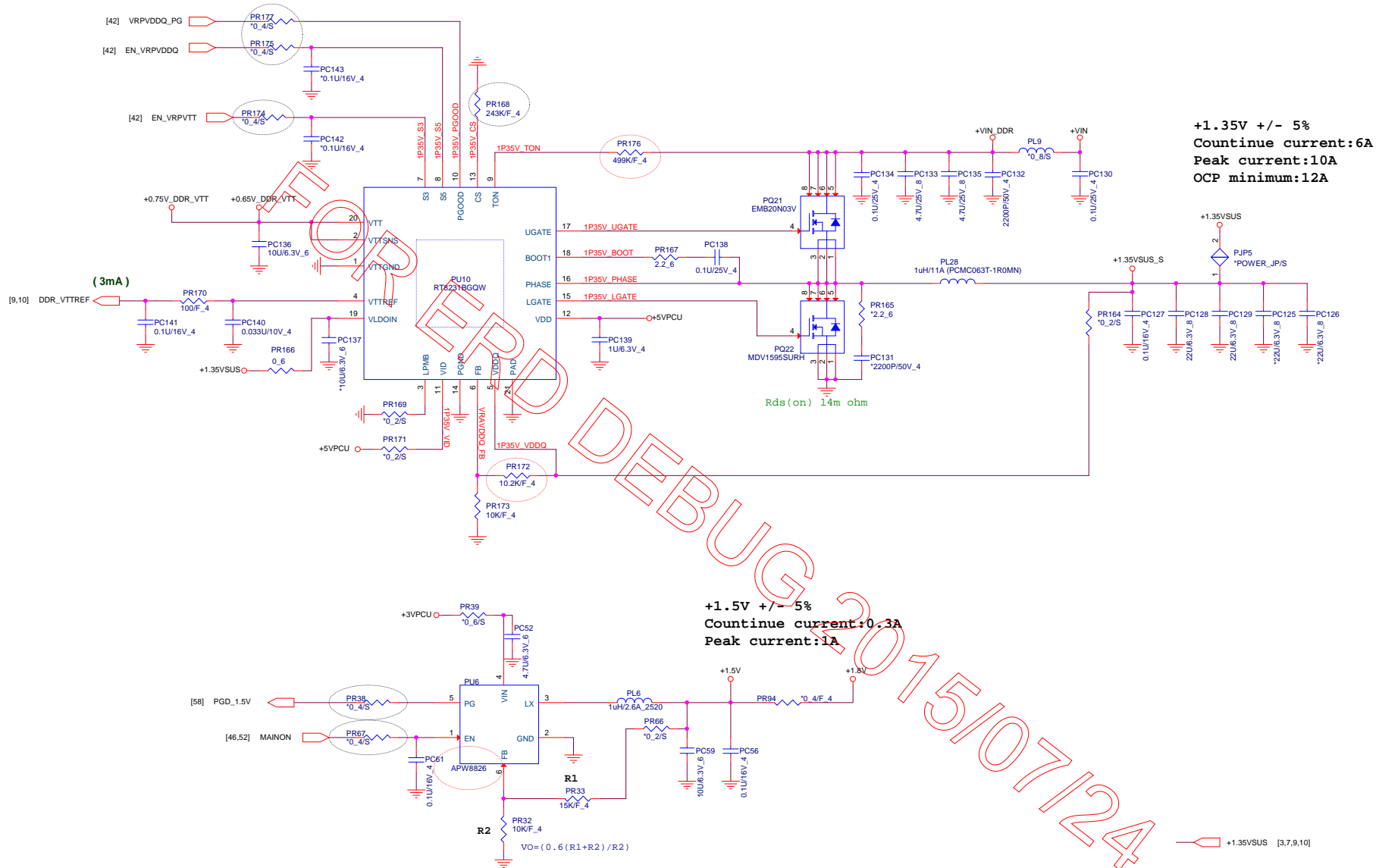
		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size Custom	Document Number 60 -- Commercial Debug card	Rev 1A	
Date: Friday, July 24, 2015	Sheet 42 of 62		


90W DC JACK

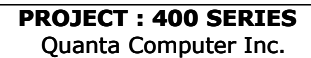
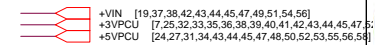
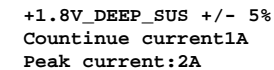




WWW.AliSaler.Com



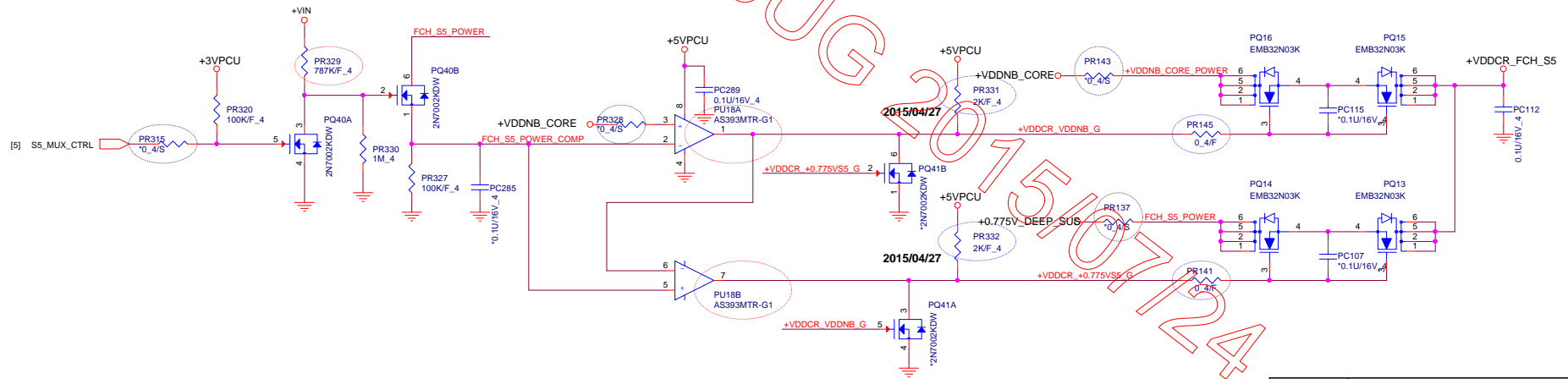
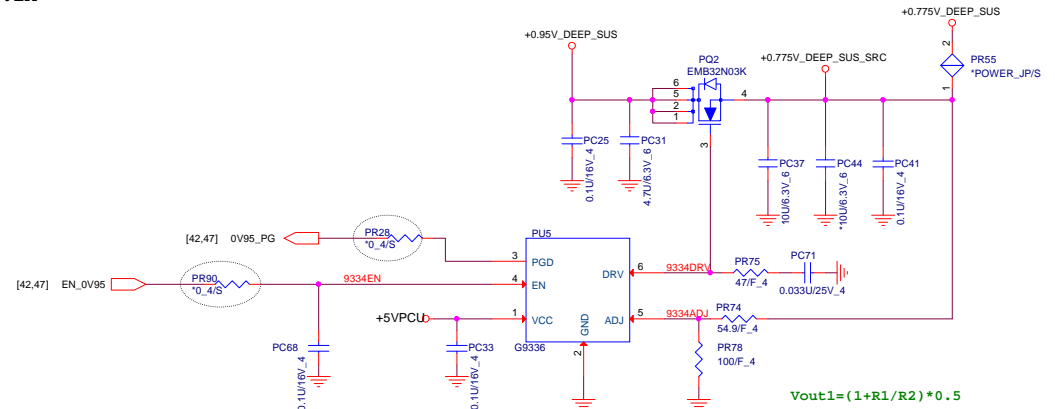
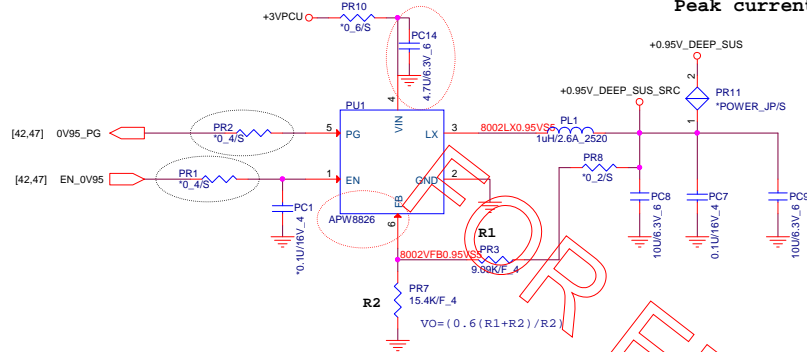
		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size	Document Number	1A	Rev
NB5	DR3 (RT8231B) 1.8V/5S	1A	Rev
Friday, July 2015	45Sheet	of 62	



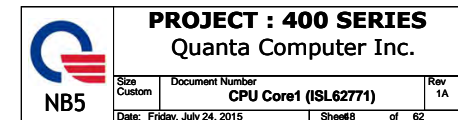
Size Custom	Document Number +1.1VS5 (RT8228)/2.5V	Rev 1A
Date: Friday, July 24, 2015		Sheet 6 of 62

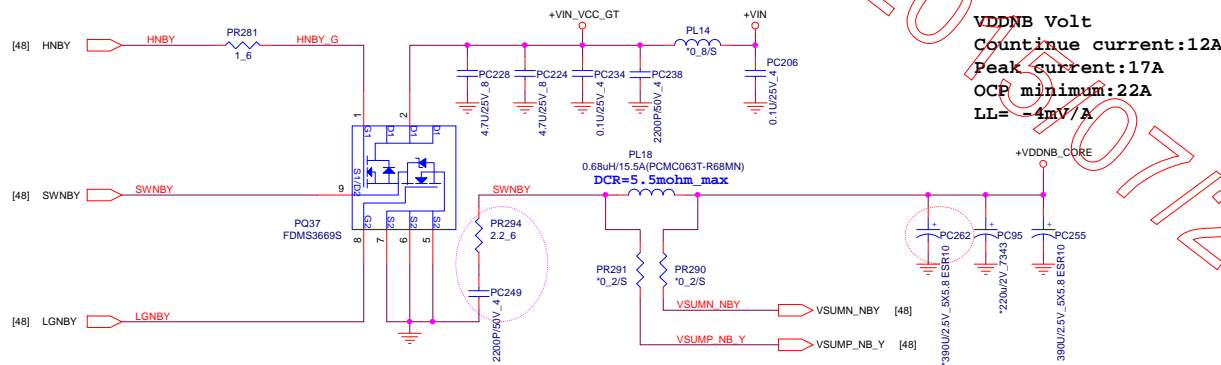
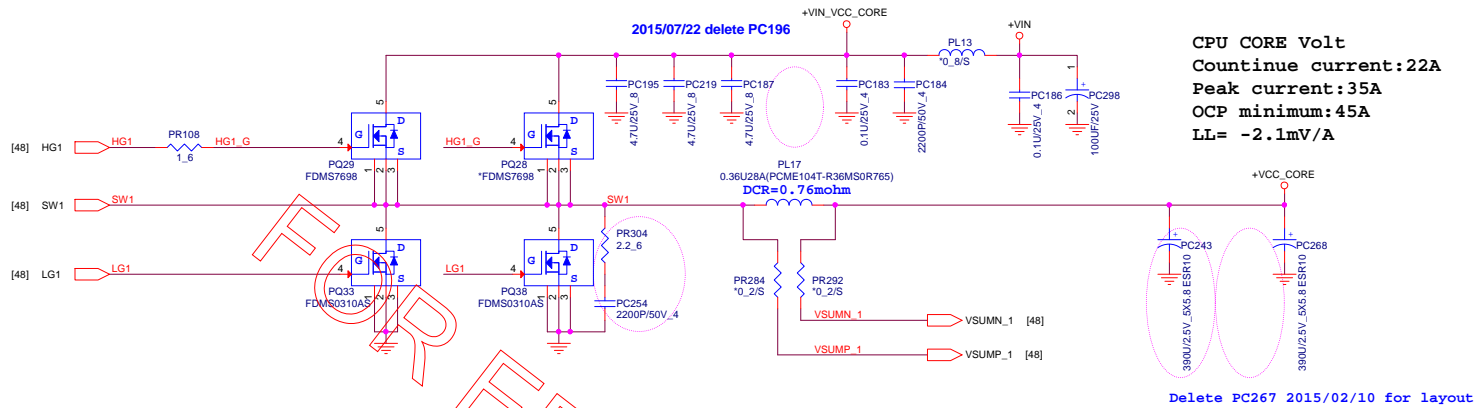
+0.95V_DEEP_SUS +/- 5%
Countinue current:1A
Peak current:2A

+0.775V_DEEP_SUS +/- 5%
Countinue current:1A
Peak current:2A



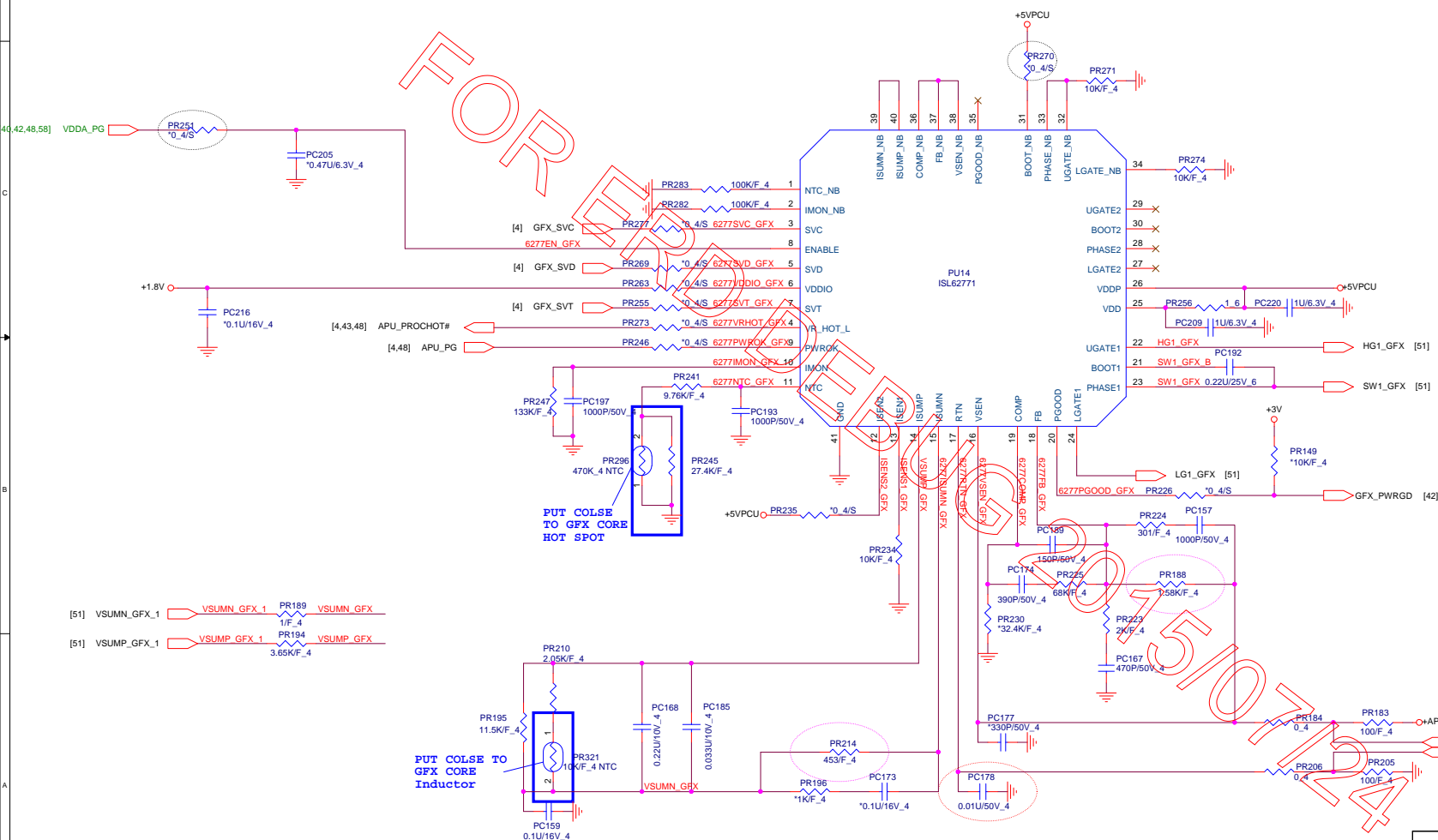
PROJECT : 400 SERIES			
Quanta Computer Inc.			
Size	Document Number	1A	Rev
NB5	+VCC_IO (NB681)		
Friday, July 2015	47Sheet	of 62	

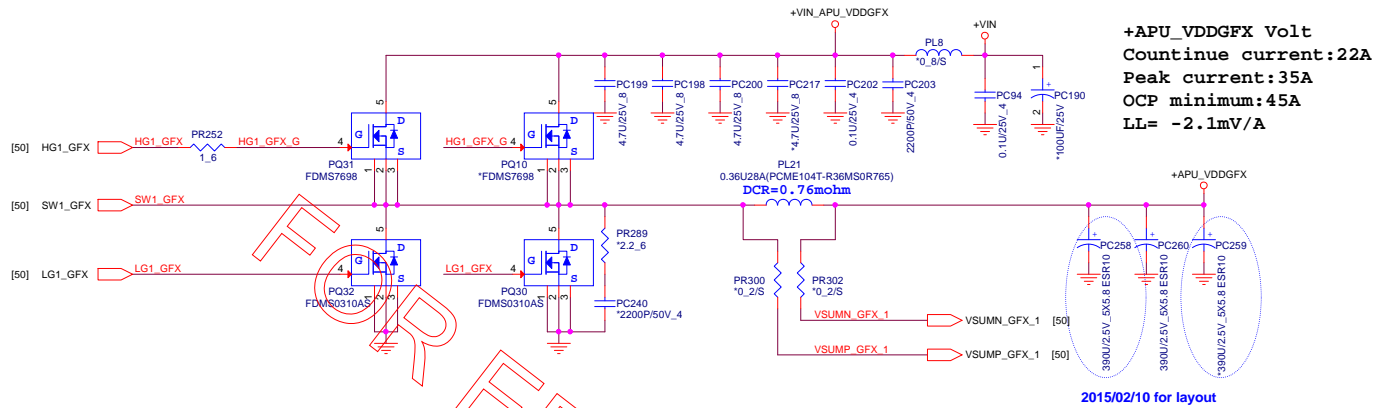





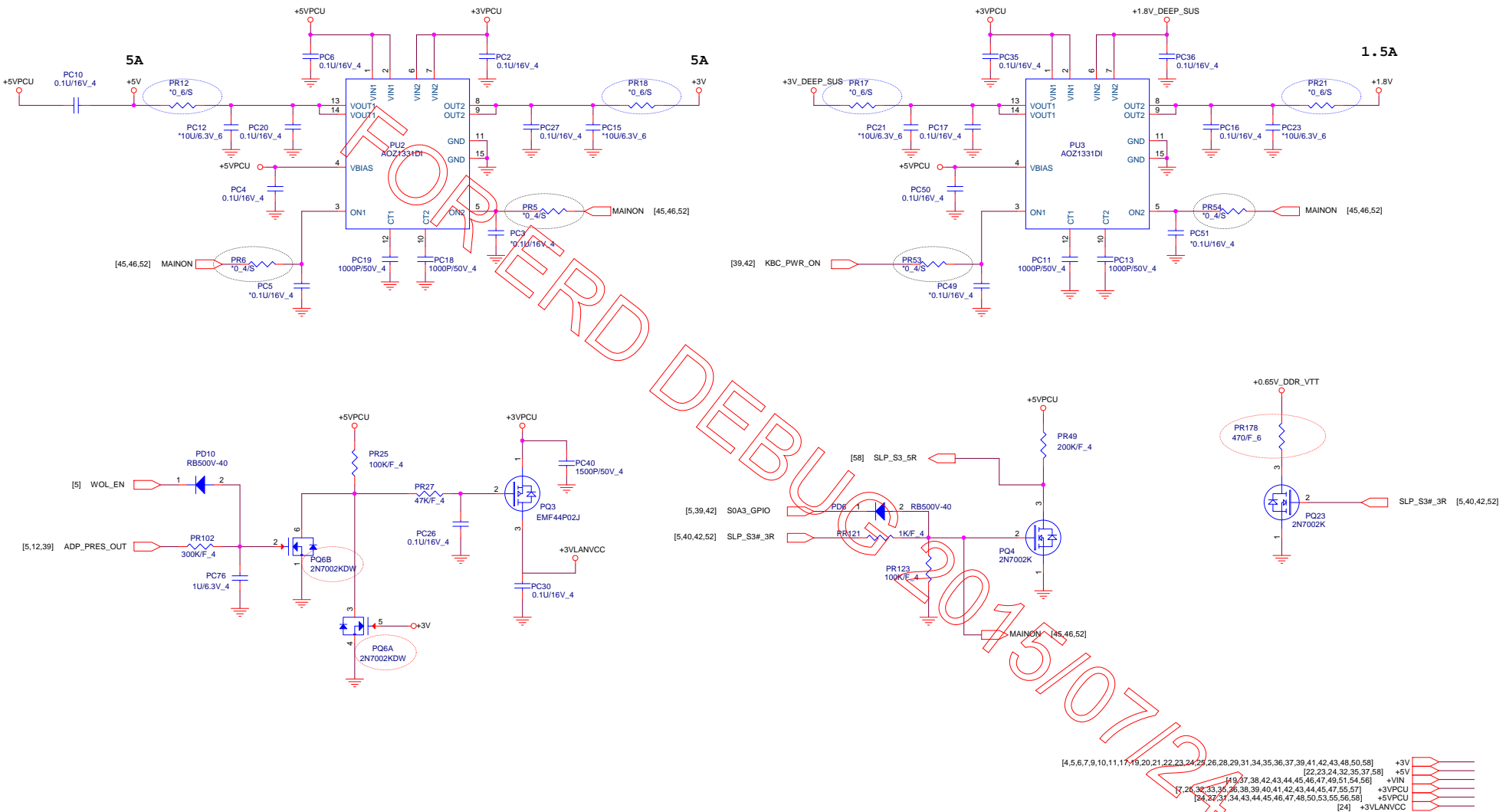
PROJECT : 400 SERIES			
Quanta Computer Inc.			
NB5	Size	Document Number	Rev
	Custom	CPU Core2	1A
Date: Friday, July 24, 2015		Sheet9	of 62

EC Charge Function	Page 38 & Page 39
Carrizo	Stuff
Carrizo-L	Unstuff



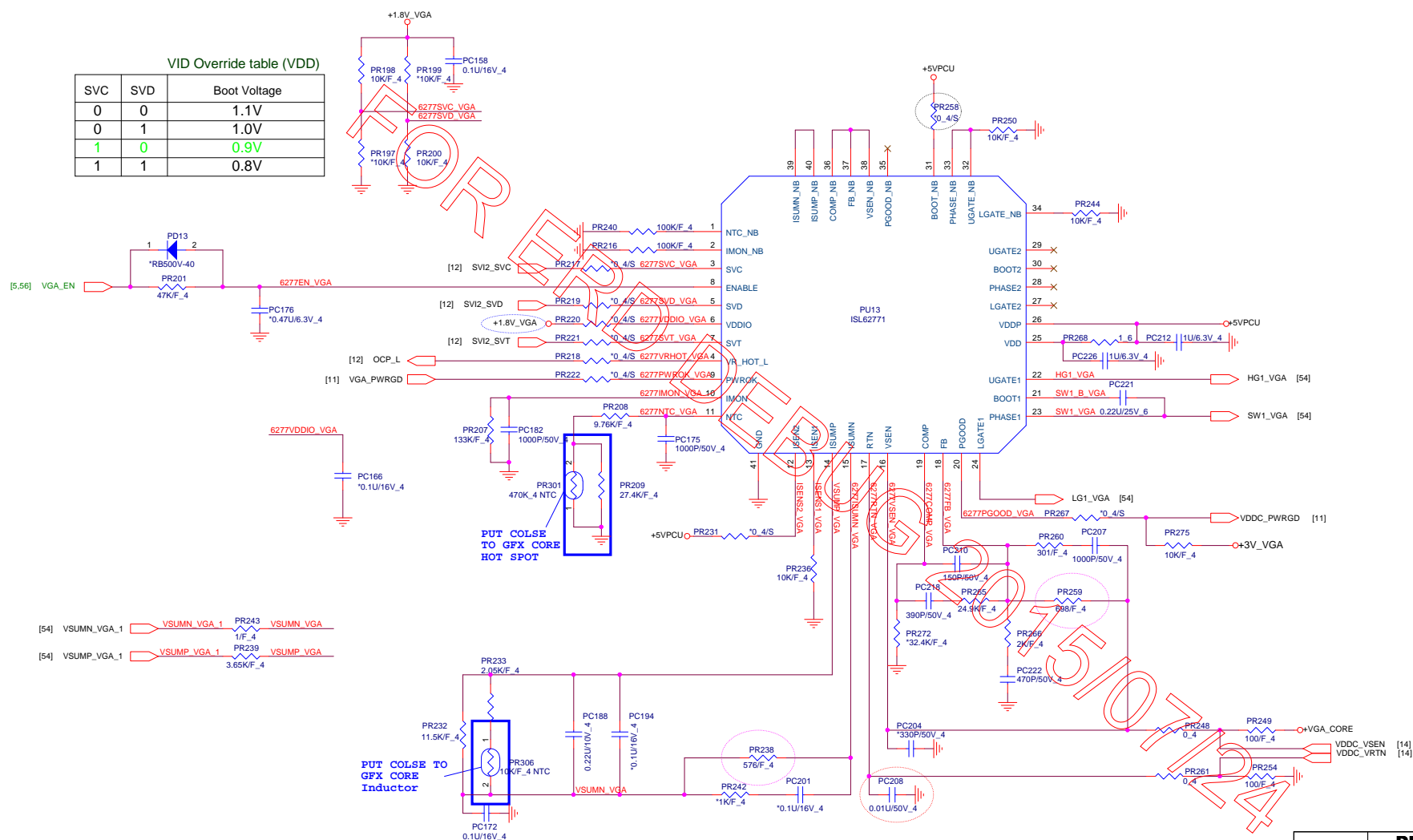


 NB5		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size Custom	Document Number	CPU Core2	
Date: Friday, July 24, 2015	Sheet 1	of	62

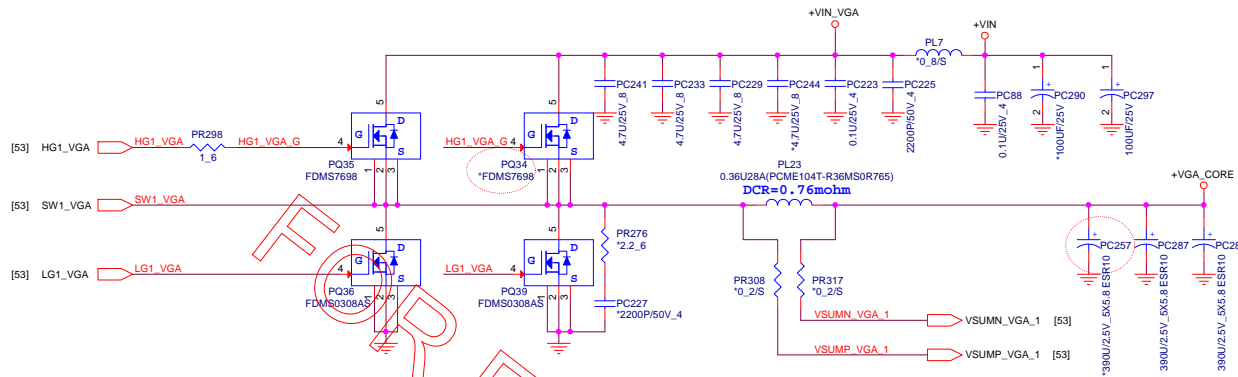



PROJECT : 400 SERIES		
Quanta Computer Inc.		
Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A
Date: Friday, July 24, 2015	Sheet 62	of 62

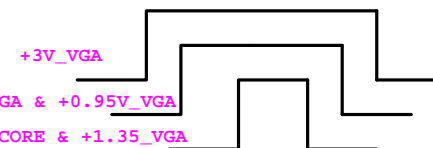
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

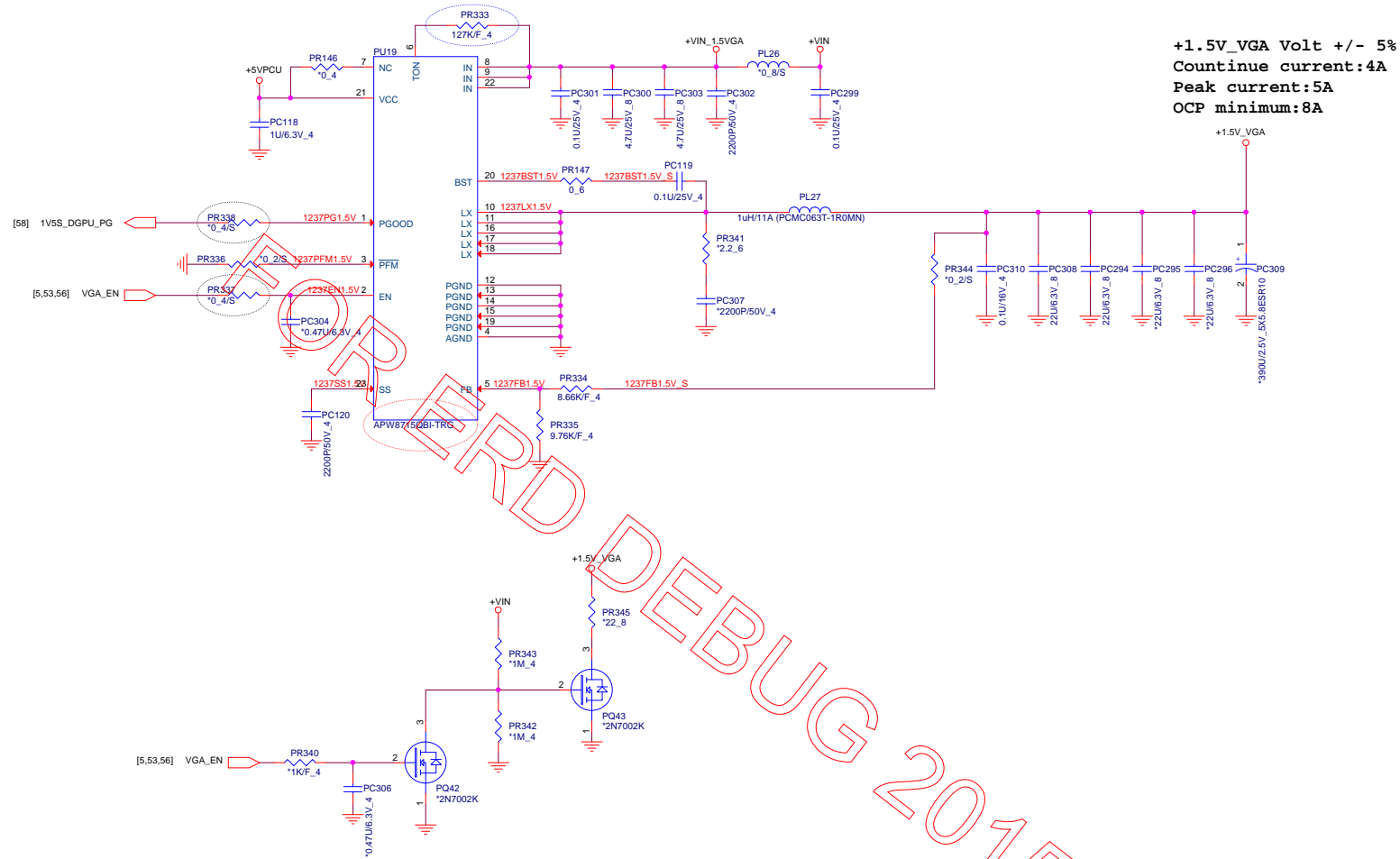



Size Custom	Document Number CPU Core1 (ISL62771)	Rev 1C
Date: Friday, July 24, 2015		Sheet 63 of 62

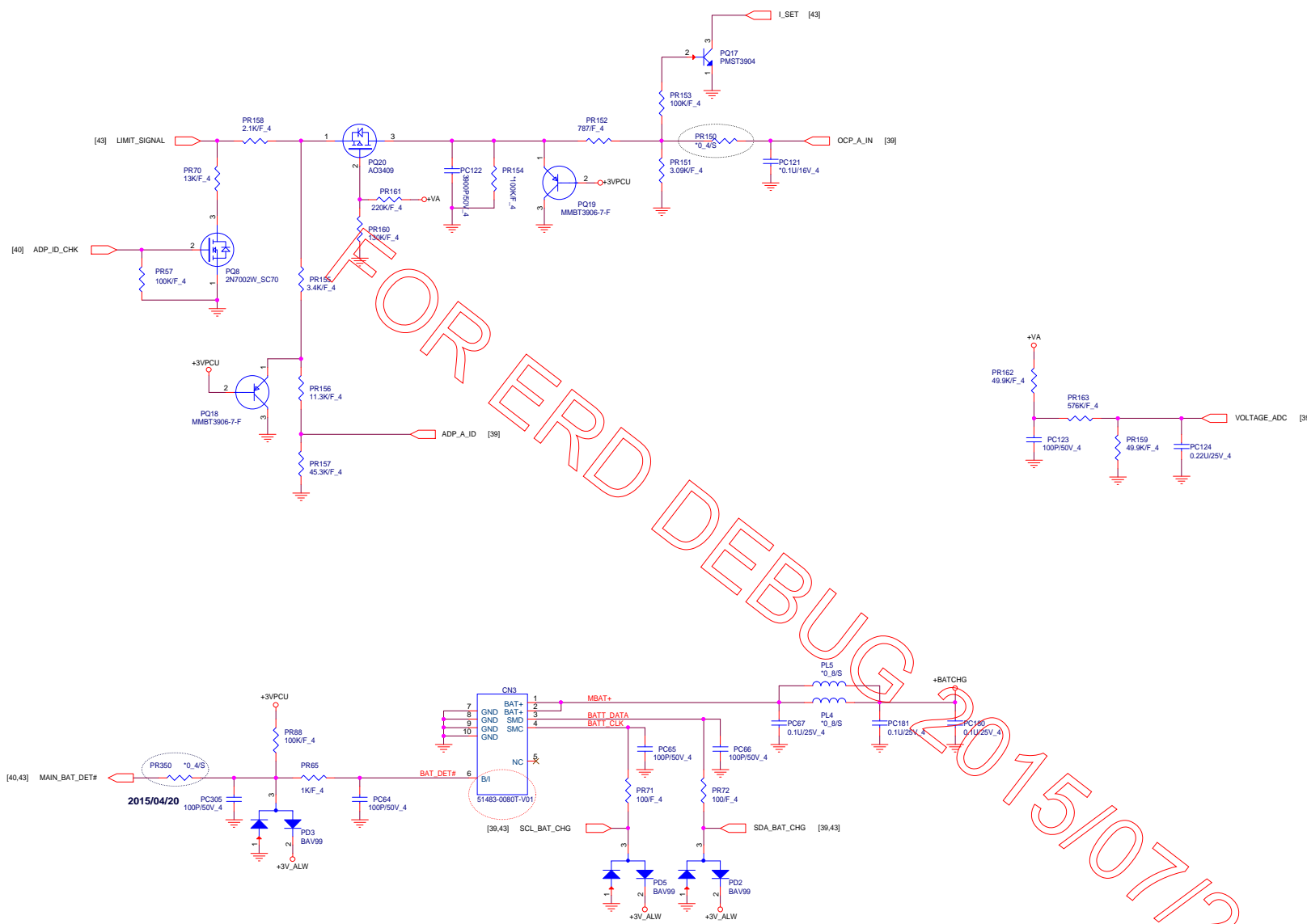


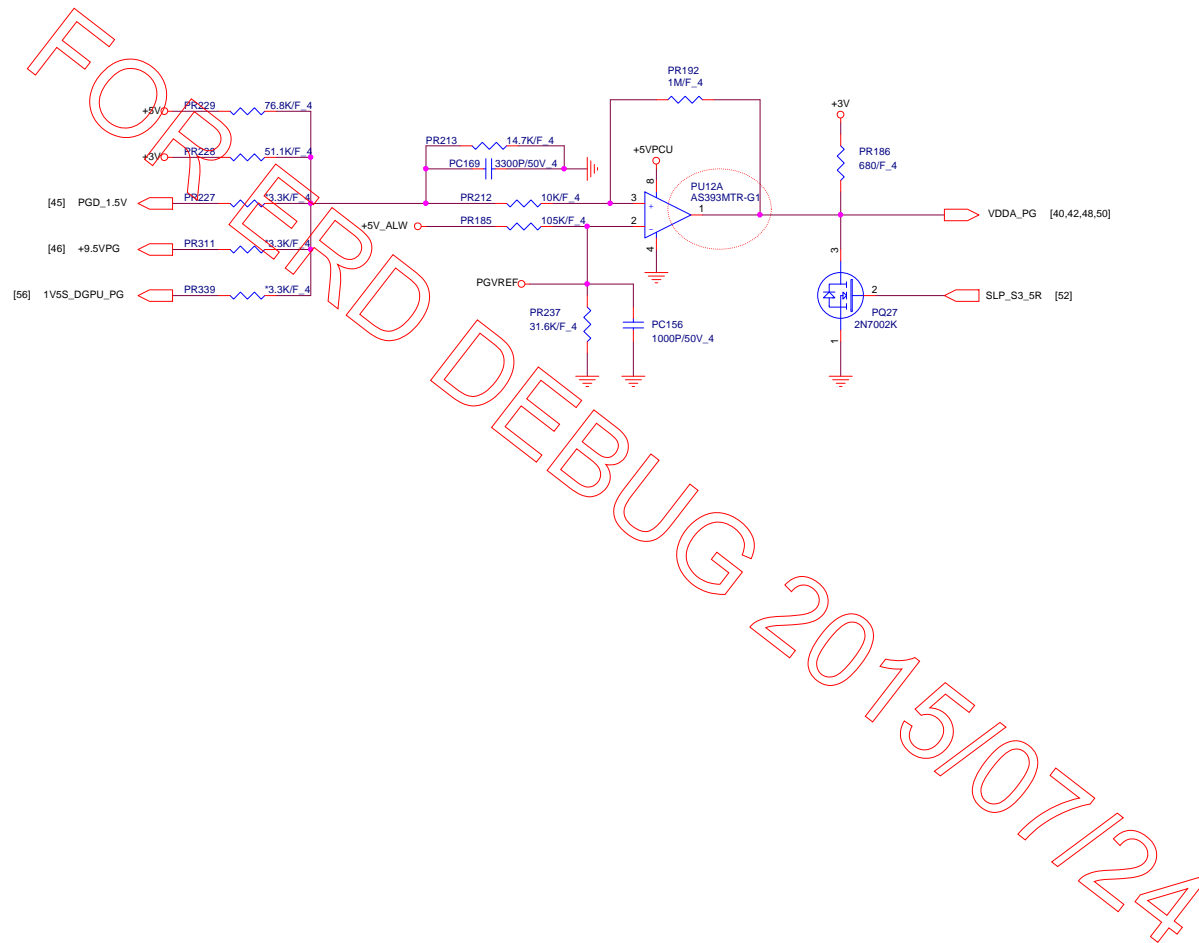
		PROJECT : 400 SERIES Quanta Computer Inc.	
Size Custom	Document Number CPU Core2	Rev 1C	
Date: Friday, July 24, 2015	Sheet 54 of 62		




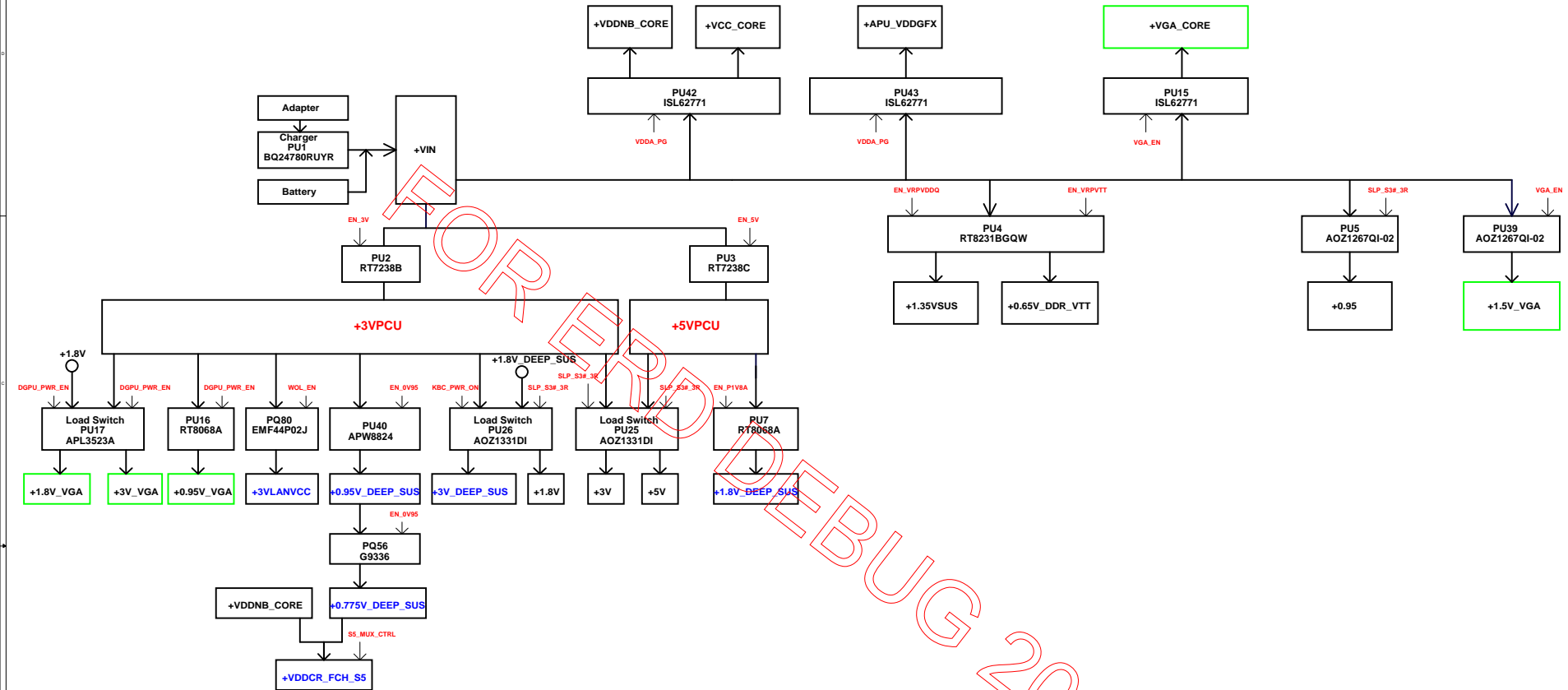


		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size Custom	Document Number +1.35V_VGA(AOZ1237)	Rev 1A	
Date: Friday, July 24, 2015	Sheet66	of 62	

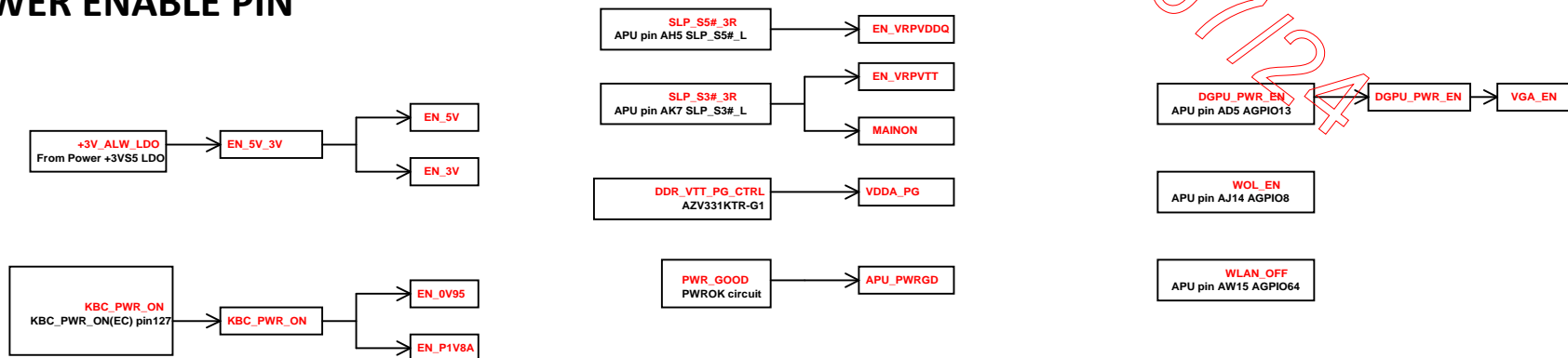


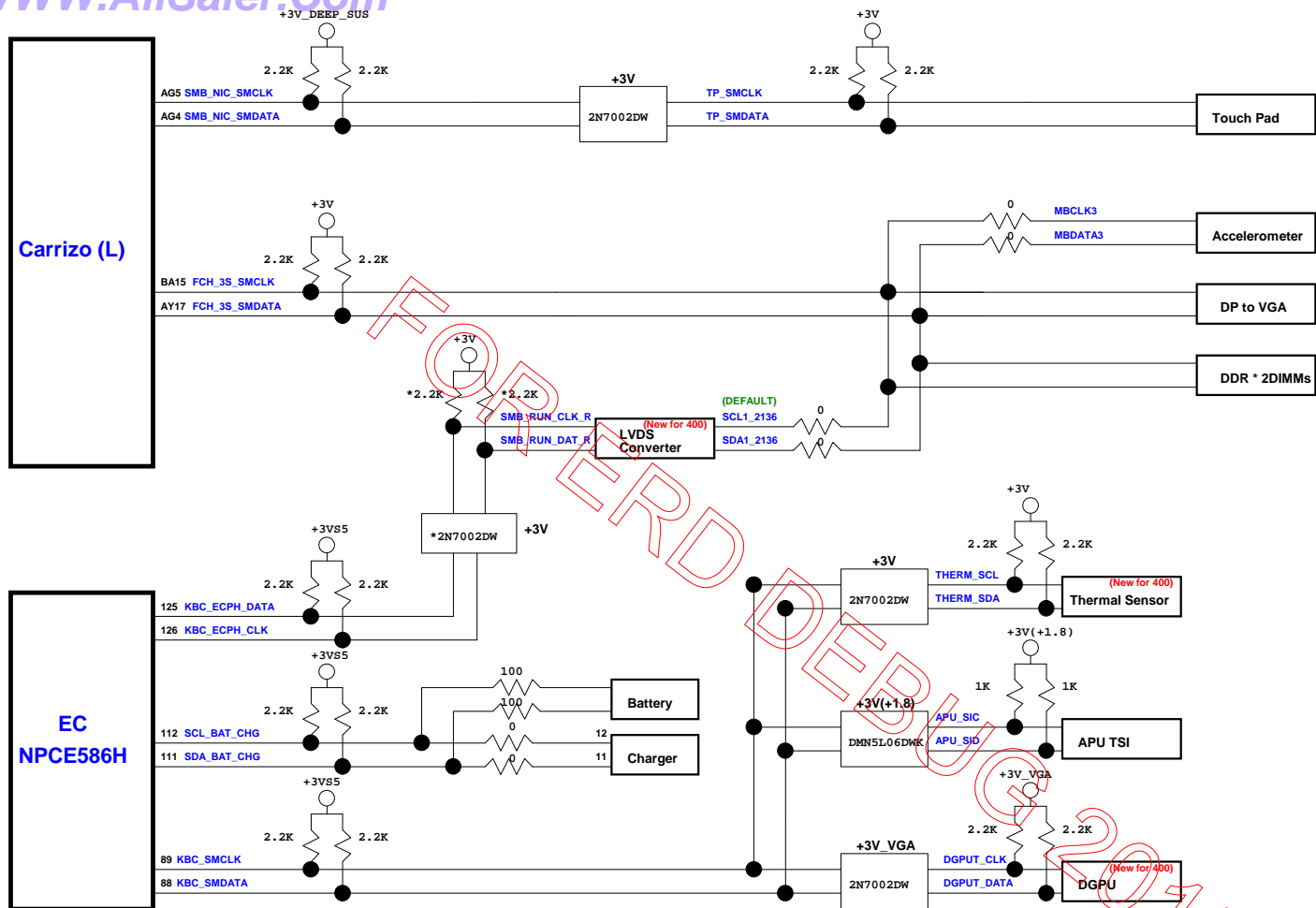


 NB5	PROJECT : 400 SERIES Quanta Computer Inc.		
	Size Custom	Document Number 56 --Power OK	Rev 1A
	Date: Friday, July 24, 2015		Sheet 58 of 62



POWER ENABLE PIN





HSIO Lane	Port Assignment
USB3 #0	NC
USB3 #1	NC
USB3 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3	USB2.0/USB3.0 Combo Jack(Left side down)
PCIE0	NIC
PCIE1	WLAN
PCIE2	NC
PCIE4	Cardreader (PCIE)
DDI0	eDP
DDI1	DP2VGA(CZ) / DP2HDMI(CZ-L)
DDI2	HDMI(CZ)
SATA0	HDD / BOM 0 ohm Option for M.2 SSD
SATA1	ODD
PEG0~3	dGPU
PEG4~7	NC

USB2.0	Port Assignment
USB2 #0	Camera
USB2 #1	USB2.0(Right side on USB Board)
USB2 #2	USB2.0(Right side on USB Board)
USB2 #3	NC
USB2 #4	Bluetooth
USB2 #5	Finger Print
USB2 #6	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #7	USB2.0/USB3.0 Combo Jack(Left side down)

[illegible][illegible]

UMA/DIS SKL TABLE

When setup the BOM, please make sure every item are finalized or not !

Schematic Value Note:

* is NO SMT part (empty)

DIS@ : for VGA mode

CZ@ : for Carrizo

CZL@ : for Carrizo-L

Function	Carrizo UMA	Carrizo-L UMA	Discrete	Page
GPU				
APU side PEG cap	NoASM	NoASM	ASM	02
GPU circuit	NoASM	NoASM	ASM	11,12,13,14, 15,16
GPU Power circuit	NoASM	NoASM	ASM	53,54,55,56
GPU enable circuit				
C143	NoASM	NoASM	ASM	05
C470	NoASM	NoASM	ASM	
D16	NoASM	NoASM	ASM	
D17	NoASM	NoASM	ASM	
Q21	NoASM	NoASM	ASM	
R160	NoASM	NoASM	ASM	
R454	NoASM	NoASM	ASM	
VBIO ID				
R76	ASM	ASM	NoASM	05
R98	ASM	ASM	NoASM	
R82	NoASM	NoASM	ASM	
R105	NoASM	NoASM	ASM	
APU VDDP GFX rail				
C122	ASM	NoASM	ASM	07
C436	ASM	NoASM	ASM	
R402	ASM	NoASM	ASM	
R155	NoASM	ASM	NoASM	